Investigation into Radiation Hardening Techniques on Differential Receiver and Power Management Unit in 0.18μm CMOS for Space Applications

by

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Declaration

This is to certify that

1. The thesis comprises my original work towards the degree of Doctor of Philosophy in Information and Communication Technology at DA-IICT and has not been submitted elsewhere for a degree,

2. Due acknowledgment has been made in the text to all other material used.

Signature of Student

Certificate

This is to certify that the thesis work entitled ***"Investigation into Radiation Hardening Technique on Differential Receiver and Power Management Unit in 0.18μm CMOS for Space Applications"*** has been carried out by Sanjay Kumar Kasodniya (201121010) for the degree of Doctor of Philosophy in Information and Communication Technology at this Institute under my supervision.

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Abstract

This report details out radiation hardening techniques, their implementation on Differential Receiver and Power Management Unit. Differential Receiver ASIC is designed with addressable, synchronous and asynchronous features called Addressable Synchronous/asynchronous Differential Receiver (ASDR) ASIC. Onboard Payload data handling subsystems use standard bus interfaces (RS422) and protocols (eg. UART) and are available in separate devices. The proposed ASDR implements the RS422 electrical interface for differential-serial-data reception and has multi-mode synchronous-asynchronous serial data handling protocol, as a single chip solution. The design has 5 bit self-address feature, which is useful if these devices are used in multi-drop configuration. Such a single chip solution is of importance for ground based application, in space and related applications. This design is fabricated with 0.18μm CMOS process. Radiation hardening techniques, guard-ring, node-splitting and differential-charge-cancellation have been implemented in the ASIC. After fabrication, the differential receiver ASIC has been tested for radiation environment specific to Single Event Effects and Total Ionizing Dose, with an aim to make it suitable for space applications. To the best of our knowledge this is the first ever integrated chip that provide interface (both Tx and Rx configuration) with protocol (UART and synchronous serial to parallel) for low speed differential data communication. A capacitive power management unit (PMU) for a DC energy harvester such as a photovoltaic (PV) is proposed. It is assumed that the input will have a minimal voltage requirement of approximately $460mV$ *and can go up to* $800mV$*, typical output from a PV cell. This is our initial attempt to design a novel PMU based on standard* $0.18\mu m$ *CMOS models to be used for applications (WSN, payload sensors) that require energy autonomy. Power management unit is designed to interface logic circuit with energy harvesters. Radiation hardening technique is used to make this design suitable for space applications. The temperature sensing system on a satellite can use ASDR and PMU for wired and wireless approach respectively.*

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Chapter 1

Introduction

1.1 Motivation

In recent times, mixed signal and analog circuit design are in huge demand for various applications of mobile communication, medical electronics, instrumentation, control, perception, multimedia etc. Because of commercial interest, processes are tuned and optimized for digital circuits, therefore it is a challenge to design mixed-signal and analog circuits using digital CMOS process[1]. In recent times, because of arrival of mobile and portable electronic communication systems, need of low power and low voltage mixed signal circuit is very high. The need for low voltage-low power in the space application is very significant considering the fact that low voltage and low power circuits need small battery and minimal heat management techniques which will effectively reduce system weight. High clock frequencies, lower technology node, increasing complexities, very low operating voltages and shrinking device dimensions, make circuits very sensitive to different kind of failures.

Radioactivity is very high in space. The functionality of most of the commercial integrated circuits is destroyed because of radioactive environment present in space. Electronic components are threatened, by the presence of particles (radiations) of different energy and nature, in the space. These radiations can damage, create undesired effects in electronic components.

They can cause 'total dose' (long term) effect which cause full or partial loss of functionality or 'soft error' (short term) effect which can be removed by power cycle.

Therefore, electronic components to be utilized in space, need special attention while designing and fabrication, their qualification processes is also specially addressed for radiation environment. The process of radiation hardening includes designing and testing of any chip or system, so that they become more resistant to ionizing radiations and minimum errors or damage is caused.

These type of ionizing radiation are present in nuclear warfare, during nuclear accidents, around nuclear reactors, high-altitude flight and environment of outer space.

The commercial grade semiconductor components do not survive in the radiation environment, so similar functionality is designed using radiation-hardening techniques, and the resulting components are called radiation-hardened components. .These radiation hardened components are designed using some design techniques and manufacturing variations so that less susceptibility to radiation is achieved. Generally radiation-hardened components tend to lag behind most recent technological developments as extensive development and testing efforts are required to fabricate a radiation-hardened electronic component.

1.2 Objective

In a typical satellite radiometer, receiver is close to antenna and its temperature is required for receiver compensation. If we want to measure brightness temperature of antenna the antenna temperature is required. Sometimes this antenna is rotating part of the satellite. This temperature sensing can be done in two ways, (1) wired and (2)wireless, as shown in Figure 1.1. In this report we have addressed both approaches with perspective of Low Power Design in Space Applications along with the radiation testing. This includes our following works:

- Novel Low Voltage Differential Current Conveyor,
- Addressable Synchronous asynchronous Differential Receiver (ASDR) Design in $0.18\mu m$ CMOS,
- Ultra Low Power Capacitive Power Management Unit in $0.18\mu m$ CMOS.

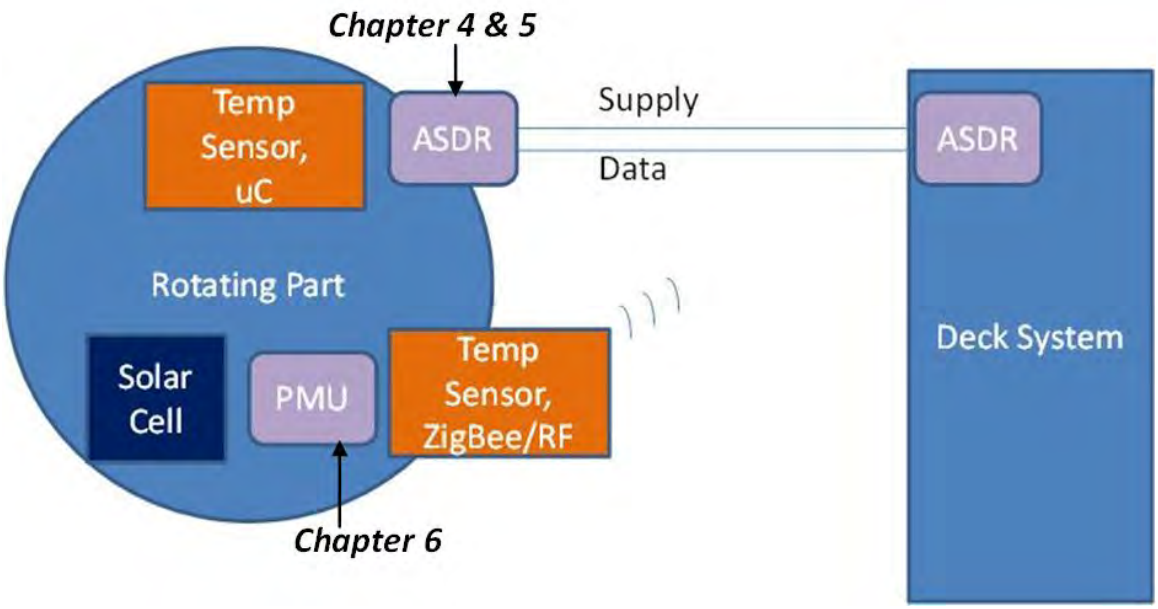


Figure 1.1: Satellite System

Our preliminary work proposes 'A new low voltage Differential Current Conveyor' circuit. It is a circuit building block designed using Low voltage current mirror technique. For low voltage applications, current conveyor (a current mode circuit) is a better option as it provides high gain-bandwidth product. The voltage independent, high bandwidth analog circuits can be designed with current-mode approach. This approach have accuracy and versatility for a wide range of applications. In this work we got insight to low voltage circuit designing by operating transistor in sub-threshold region.

Our other work involves designing of Addressable Synchronous asynchronous Differential Receiver (ASDR). ASDR implements the RS422 electrical standard for differential-serial-data reception and has multi-mode synchronous -asynchronous serial data handling capability. The 16-bit parallel

data can be generated from this serial data. Combination of these functionalities is not available commercially in a single chip and hence a single chip solution is designed. This design is fabricated using $0.18\mu m$ CMOS technology and is packaged. Radiation hardening techniques of guard-rings, node-splitting and differential-charge-cancellation have been used in this design to get better radiation performance. TID and SEE/SEL testing is also done and results are satisfactory. Here we have used native transistors to increase voltage headroom. Radiation hardening techniques of guard-rings, node-splitting and differential-charge-cancellation have been used in this design to get better radiation performance.

At present temperature of rotating part to deck part of satellite is taken by wires through slip rings. There are two wires, one for power and other is for data. It can be done wireless, power from energy harvesters (solar, vibration), temperature data over RF wireless link (ZigBee), as shown in Figure 1.1. Power from energy harvester need to be regulated by Power Management Unit (PMU). The aim of our later works is to design and develop a PMU, which takes power from solar cell and provide enough energy to operate sensor, micro-controller and RF circuits. PMU may need to double the voltage if its not sufficient to operate the circuits and regulate the supply voltage with minimum power consumption. PMU will store energy in capacitor and it will be used by micro-controller to read the temperature from sensor and send it through RF link. Once capacitor is discharged PMU will again charge it with required voltage. Our work is up to designing the circuit components of ASDR and PMU, the complete system can be designed using them and is in the scope of future work.

1.3 Chapter Layout

This thesis contains seven chapters. The motivation and objective of this thesis have been mentioned in *Introduction*, the first chapter. In the second chapter, *Literature Review* is discussed. The *Radiation Effects and Mitigation Techniques* is the study work, which has been discussed in detail in third chapter, where it is shown how radiation affects circuits and how they

can be mitigated. The *Addressable Synchronous asynchronous Differential Receiver (ASDR) Design in* $0.18\mu m$ *CMOS* implementation has been covered in fourth chapter. *Radiation Test Results* of ASDR has been given in fifth chapter. The *Ultra Low Power Capacitive Power Management Unit in* $0.18\mu m$ *CMOS* is discussed in sixth chapter, where the circuit works in sub-threshold region. *Conclusion and future work* is the last chapter. The *Novel Low Voltage Differential Current Conveyor* is our preliminary work, which has been discussed in detail in Appendix, where it is shown how and why sub-threshold operation is suitable for low voltage applications.

Chapter 2

Literature Review

The space environment is outside the atmosphere of the earth, which is beyond 100 Km from the surface of the earth [2]. The authors [3] have described various aspects of radiation environment *i.e.* electromagnetic radiations of the range X-ray and gamma-ray, trapped charged particles, neutron, cosmic rays, magnetic fields and high vacuum. Effects of these radiation on electronic parts is also discussed, where analog circuitry is widely affected by total dose (charge accumulation) compared to digital part which is more affected by transients. Authors have described various electronic parts and threshold of radiation-damage for them. Semiconductor devices are susceptible to radiation effects and care must be taken while using them in space. For maximum reliability at higher temperatures, silicon semiconductors can be used but in terms of the radiation tolerance, germanium-semiconductor may be better.

Space radiation environment is described in terms of trapped and not-trapped charge particles. The authors in [4] have discussed the effect of trapped particle in Van-Allen belt and South Atlantic Anomaly (SAA). Radiation environment of space put lot of constraints on spacecraft electronics design. This issue can be addressed by radiation hardening circuit design techniques, few process variations, selective part placement and proper shielding against ionizing radiations. And hence systems with high performance and long endurance can be realized.

The effect of radiation on an electronic component and the consequent degradation in performance of devices, depend upon the function of the device and physical principles behind it, the type of material, the rate of energy deposition in material and type of radiations.

Ionization and atomic displacement are two main types of interactions, which radiations can have with materials [5]. Single Event Effects (SEE) or Single Event Phenomena (SEP) is also an ionization effect, and the terminology is adopted from NASA-JPL depicting SEL or 'single-event-latchup' as well as SEU or 'single-event-upset'. Single Event Effects (SEE) is an instantaneous phenomenon. Once SEU is identified it can be corrected by applying reset and is often temporary in nature [6].

TID is a charge cumulative effect over a period of time, affecting the threshold voltage of MOSFETS to an extent that these are either always in 'on' condition or in 'off' condition [7] [8]. This will lead to catastrophic failure and permanent loss of functionality.

The ionizing radiation creates electron hole pair in the semiconductor, they are drifted by electric force, and result in a pulse of current. If the charge of electron-hole pairs created by ionizing radiation near a sensitive node in a memory (flip-flop) element exceeds the critical charge Q_c, which is needed to alter the logic level of the memory element then upset will be there. The vulnerability to SEU increase with smaller device geometries and evolution of technology as the critical charge Q_c also decrease with scaling [9], while its better for total-dose point of view as less oxide volume is available for charge trapping.

Single event latch up can have a catastrophic effect on device, as it can be there for a long time and can be destructive. Parasitic resistor and BJT in CMOS technology are the main reason behind single event latchup. Bulk CMOS structure contains parasitic vertical and lateral bipolar pnp and npn transistors which forms pnpn thyristor. When current spike created by ionized electron hole pair, is more than a certain level, the thyristor will turn on and a low resistance path will be there between supply and ground pins. This low resistance path can create large currents between VDD and VSS. This can lead to local heating and even burnout of the device, and complete

functionality of the circuit will be lost.

In order to avoid latch up, the thyristor triggering condition can be avoided in CMOS process by decoupling parasitic BJTs [10]. There are several ways to decouple the parasitic bipolar transistors and reduce the parasitic resistance like deep trenches (STI), silicon-on-insulator, retrograde wells, use of epitaxial layers, etc. These techniques will increase the production cost. Unless it is required these techniques will find minimum use and standard bulk CMOS processes is used.

'Radiation hardening' derived from military terminology, which require to survive the (a)transient effect of an intense burst of gamma rays neutrons at a dose rate at least 10 billion times higher than that experienced in space and (b) the long lived effects or 'total dose' received from this burst. Different environment require a different approach to hardening. A spacecraft designer may consider a level of 100 krad tolerance to be 'hard', a military designer may apply the term 'hard' to megarad tolerance only.

Fabrication of a typical CMOS integrated circuit require large number (several hundred) of processing steps. Many of these processing steps can influence susceptibility of a device in radiation environment. As most of the charge is trapped in oxide and silicon-oxide interface, processing steps involved for them are more critical. Wells preparation, oxide growth, cleaning, wafer preparation are some of these factors which plays important role in making the device suitable for radiation environment.

Epitaxial layer on substrate is another alternative to bulk substrate. It is a thin mono-crystalline film which is grown on the substrate. The lattice orientation and structure of the deposited film remains identical to that of the substrate as the same acts as seed crystal. Epitaxial layer of 2.75 μm thickness is good enough for mitigation of latchup [11], [12].

One way of doing radiation hardening by process is by Silicon-on-insulator (SOI) technology. The effect of SOI process on dose-rate, single event effects and total dose are discussed in [13]. The benefit of silicon-on-insulator is that transistors are fabricated in thin layer of silicon on the top of insulating substrate, hence less volume is available for free charge generation (ionization), which helps in SEU mitigation. Because of the thin silicon layer, parasitic

capacitance as well as p-n junction area, both are considerably less. Bulk-silicon devices have less complex total dose response compared to silicon-on-insulator devices which have insulating oxide layer buried under silicon layer. The ionized charge can be trapped in buried, insulating, oxide layer as well, which can deteriorate its radiation characteristics.

Apart from LOCOS (LOCal Oxidation of Silicon) the Shallow Trench Isolation (STI) is another technique for device isolation. It is used to prevent leakage between two adjacent transistors. In lower CMOS technology nodes (sub-0.5μm), generally STI is used for isolation as it takes less area on the die compared to LOCOS. STI also removes problem of 'birds beak' present in the LOCOS process, and hence more widely being used as a method of isolation. The authors [14] found that very less ionized charge is present on the top of the trench, as positive gate bias produces vertical electric field which pushes the charge down the trench.

During a single event strike, the charge collected by 'triple well' devices is more compared to the charge collected by 'double well' devices [15]. In a triple well technology, the p-well potential will rise when holes are accumulated in p-well. The charge accumulation in the p-well can be reduced if p-well contact area is increased. Large number of well contacts help in decreasing charge accumulation in the well.

To reduce the impact of radiation, the Enclosed-Layout-Transistors or Edge-Less-Transistors (ELT) are used in place of standard rectangle transistors layout. As thick field oxide (STI), is situated nearby gate oxide, and has larger tendency to capture free charge, it can affect overall control on transistor. In Edge-Less-Transistor, the gate is completely surrounded by source or drain, no field oxide is available near the gate. This technique has advantage of no birds-beak leakage effect on device. Furthermore this technique reduces TID effect and it improves SEU performance [16]. The ELT's model and behavior is complex and it require large area. In this technique there is a limitation in aspect ratio available for design as any random aspect ratio can not be implemented. Because of its complex structure, ELT is difficult to model it and lot of work has been done on that [17].

To prevent the latch-up, use of several guard ring structures have been

analyzed by authors [18][19]. Guard ring around MOSFETs have been found to be very effective against single-event-transients (SETs) [20]. In this layout method parallel contacts are placed between source-substrate[1] and between drain-substrate[2]. Guard ring structure helps in removing the ionized charge from drain/source area to VDD/VSS through low resistance path. Because of multiple taps in guard-ring, parasitic resistance is drastically reduced and the voltage developed across these resistors will not be enough to trigger the thyristor [18].

To design a more radiation tolerant storage element, DICE (Dual Interlocked storage CEll) based architecture is discussed in [21]. DICE architecture can be implemented on standard commercial CMOS process and radiation hardening can be achieved. There are ten MOSFETs used in a DICE based latch. It offers high operating speed and lower power dissipation compared to other radiation hardening architectures. The effect of parameter variations and transistor size ratios on DICE architecture is very less.

In computer systems, the Triple Modular Redundancy (TMR) technique is being used for improving reliability, since a long time. TMR is being used in circuit design topology for radiation hardening. Around three times area is used in TMR solutions, and hence they consume more power. The authors in [80] have discussed techniques to reduce power consumption in TMR-based architectures.

Usage of 'C-element' and 'storage elements redundancy' is another way to achieve robustness in flip-flop against SEU [23]. This flip flop has dual redundancy unlike TMR where triple redundancy is implemented. This architecture occupies less area compared to TMR architecture where triplication is required. Standard digital design flow can be used, if these cells are added in the standard cell library.

Errors in data can be detected and/or corrected by incorporating Forward Error Corrections (FEC) or Error-Correcting Codes (ECC) algorithms. These codes append few redundant or parity bits in to original data bits. While writing in to memory, data is passed through an encoder, which in-

[1]or source-well in case of NMOS
[2]or drain-well in case of PMOS

troduces some redundant bits (parity) in the data. While reading back, the data is passed through a decoder. The decoder determines if there is any bit flip and corrects that bit. Most commonly used error correcting codes in space and aeronautic applications are Parity checking, Cyclic Redundancy Check, Turbo , Reed-Solomon, and Hamming codes [24]. Different codes have different capability to detect and/or correct the error in data. Error correcting codes are of two types: convolution codes and block codes. In data-storage applications, block codes are used while in data-transfer applications, convolution codes are used. Block codes can be of two types, either they can only detect the error or they can detect as well as correct the error in the data. The capability of the error correcting codes depend on the number of redundant bits. All error correcting codes have disadvantage of time-overhead[3] and area-overhead[4].

Another layout design technique of radiation hardening is Differential Charge Cancellation (DCC). The charge, which is responsible for single event transient in differential circuits, is shared and converted in to common mode signal, which in turn rejected by constant tail current of differential circuit [25]. The single ended error signal is converted in to common mode signal by a simple change in layout. Generally, source terminals of differential pair transistors are kept nearby, while in this technique drain terminals of differential pair is kept close, so that any transient on drain nodes become common to both the transistors. Keeping source terminals of differential pair close in layout is not useful as they are anyhow connected and any transient at source node is already a common mode signal. This layout technique does not have any area or matching penalty compared to common-centroid layout. Radiation sensitive area is drastically reduced if this layout technique is used and it is more effective in lower technology nodes.

Continuous-time analog/ mixed signal circuits and switched-capacitor circuits can be hardened against single–event–effects, by creating parallel signal paths known as 'node splitting' [26]. It is a radiation hardening by design technique at circuit/architecture level. The circuit is split/peeled in such a

[3]To compute redundant data bits and check original data for consistency
[4]To store redundant data bits

way that internal nodes are parallel sub-circuits paths which are shorted at output and input node. Electrical performance of the original un-peeled circuit is maintained at peeled level by proper transistor sizing of sub–circuits. When ionizing radiation strikes and tries to upset one sub-circuit, while other sub-circuits will behave normally and will nullify the effect of transient at output. Hardening via node splitting technique can be implemented in two ways: peeling only sensitive nodes (smart peeling) or peeling all the internal nodes[5].

The source, most commonly used for testing of ionizing effects in silicon components or materials, is Cobalt-60 (^{60}Co). It has a half life period of 5.27 years. It emits radiation in the energy band of 1.332 and 1.173 MeV [10]. The ^{60}Co is produced from inactive ^{59}Co by heavy neutron irradiation in a reactor. In a typical irradiation chamber, a cylinder of ^{60}Co, sealed in a steel jacket, is placed in a thick lead shield or concrete cell. Electronic components arrayed in sockets in circuit boards are kept inside steel jacket of the ^{60}Co source. Radiation response of the circuit can be monitored through wires. All electronic beams act as a source of ionization, but only the high energy machines (particles of energy considerably greater than 1MeV) will produce displacement damage in semiconductor.

An electron beam, accelerated by the field between earth and an electrode (charged to a very high static potential), is used for SEE tests. The charging is accomplished by means of a moving belt which carries charge from a DC generator to the insulated 'head' electrode. In this way potential of around 10 million volts can be produced. Electrons released from the electrode are accelerated away from it down an evacuated column and emerge through a titanium vacuum window as a beam of about 2 cm diameter. A device can be placed in this beam for tests related to Single Event Effects (SEE).

The voltage independent, high bandwidth analog circuits can be designed with current-mode approach, which exhibit good performance, accuracy and versatility for a wide range of applications. Several applications[6] using second generation current conveyor (CCII) are described in literature [27, 28, 29].

[5]Massively Multiple Peeled Layout (MMPL)

[6]like oscillators, amplifiers, filters etc.

Because of their limited gain-bandwidth product, conventional op–amps are not used in the high-frequency applications. In the high–frequency circuit-designs, current-mode circuits are widely used. The Current Conveyor (CC) has been proved to be an important part of current mode design. The current conveyors are commercially available (AD844) and can be used in instrumentation amplifier, filters, DC-to-DC converter, electrical impedance tomography, high-frequency precision rectifiers and RF mixers.

Differential–difference–current–conveyor (DDCC) was introduced by Chiu et al [27]. Author has combined the advantages of the CCII (second Generation Current Conveyor) and differential difference amplifier (DDA), making a new circuit named DDCC. It has been shown that rather than CCII and DDA based circuits, DDCC based circuits provide better design choice.

RS422 is a well accepted electrical interface standard for low speed differential data communication for payload data handling (PDH) subsystems on a satellite [30, 32, 33, 31, 35, 36, 34] whereas LVDS is used for high speed differential data communication [31]. Satellites have payload data handling (PDH) subsystems to ease the load on the on-board data handling (OBDH). For robust data communications among payload subsystems, differential transmission is an obvious choice. Authors in [32] have discussed the advantages of the wireless approach for on-board communication. The wireless approach has advantages viz. (1) flexibility in connectivity, (2) no harness requirements, (3) ease of assembly, integration and testing. However this approach has issues related to electromagnetic interference (EMI), reliability, robustness and power constraints. Furthermore space qualified components are also not available to enable wireless connectivity and hence the wired (RS422) approach is the natural choice. Authors in [33] have discussed the design of payload data handling system for a satellite where RS422 interface devices with UART protocol is implemented on an FPGA (Field Programmable Gate Array). The two separate devices used for asynchronous serial data communication are proprietary, hence difficult to adopt. Authors in [34] have discussed spacecraft distributed control system based on RS422 interfaced to a micro-controller, which has an inbuilt UART. The system is similar to [33] where two separate devices are used for asynchronous se-

rial data communication. It is evident that on-board payload controller use serial communication extensively and this serial protocol has to be either supported by a micro-controller (MCU) or an FPGA. At the PDH, FPGA or MCU based solution is useful as it can support multiple functionalities in tracking telemetry, thermal control and altitude control [33]. However the other end of the data link, based on these devices, as multi-chip functionality is often not required and the available systems are therefore expensive. In complex multi-mode imaging radars, serial to parallel conversion is frequently required. Although shift registers can perform this operation with commercially available differential transceivers, these designs are often less useful for space related applications since the discrete devices are often resource-intensive and pose reliability issues [37, 38]. Reliability, power and area remains a challenge for space related applications and are of prime importance. In these devices, features such as addressable, device-selective transmissions on multi-drop or daisy-chain on a common bus can provide ease of connectivity [39]. Additionally auto-baud detection can accommodate different subsystems with different baud rates [40], often a necessity. To the best of author's knowledge, there is no integrated solution available that combines the above mentioned features for serial communications.

Energy Autonomy in battery less systems and wireless sensor nodes is gaining a lot of attention from researchers [41] working on ultra low power systems. Energy harvesting techniques are the key to attain energy autonomy for these electronic systems. There have been numerous efforts discussing AC (piezo, vibration) and DC (solar, thermal) energy harvesters that produce useful quantities of energy driving low power electronic systems [42]. Mostly the low voltage output from these harvesters is not sufficient to drive the electronics, and require up conversion. Dedicated power conversion and power management circuit is of utmost importance in such harvesting circuits [43]. The key to such power management unit (PMU) is low power consumption, high efficiency and fewer number of off chip components. Both inductive [44] and capacitive methods [45, 46] exist and offer elegant solutions for these energy harvesting electronic circuits. The works described in [16-21] also emphasize the importance of capacitive energy harvesting methods. For ex-

ample, in [47, 48, 49] authors have demonstrated the power management unit that operates at very low voltage (120 mV) and very low power (sub-μWatt) that can be useful for several applications including wireless sensor nodes. Authors in [50, 51] have discussed their long efforts on energy harvesting circuits and their application. We looked at PMU from power and space applications point of view.

Chapter 3

Radiation Effects and Mitigation Techniques

3.1 Introduction

Space environment consist of harsh radiations, composed of various energetic particles, and hence electronic components being used in space, need a different approach during their design, fabrication and qualification [52].

Different type of undesired effects are seen in the semiconductor devices, because of diverse nature and energy of these space–radiation/energy–particles [53], [54], [55], [56]. The effects can be of two types, one is instantaneous effect, which is cleared by supply reset. The other effect is accumulation effect, resulting in to performance degradation with time and ultimately may lead to catastrophic failure.

The process making semiconductor devices immune to errors and failures caused by ionizing radiations[1], is known as 'radiation hardening'.

Radiation hardening can be achieved by either process or by design or by both. Radiation hardening by process is achieved through specific foundries having special processes[2] and because of these special processes, the cost of component is very high. The demand for space grade components is not much

[1] High-energy electromagnetic radiation and energy particle

[2] Like silicon-on-insulator or silicon-on-Sapphire, epitaxial layer

and hence driving force behind these processes is not there. Therefore less technological progress is there compared to standard CMOS process which is state of the art. The another approach, which is radiation hardening by design is more popular now a days in which standard CMOS process is used. The radiation hardening by design is achieved by changing architecture[3] and layout[4]. This chapter is heavily adopted from the ESA handbook on *"Space engineering, product assurance techniques for radiation effects mitigation in ASICs and FPGAs"*[57].

3.2 Source of Radiation

Radiation is defined as the process in which energy is emitted as particles or waves. The primary source of these radiations are cosmic rays, solar flare, trapped protons and trapped electrons[2].

3.2.1 Radiation : Trapped Particles

Charged particles, of different energy, coming from cosmic rays and solar wind, are trapped in earth's magnetic field. These trapped charge particles form the radiation belt around the earth. Mainly protons and electrons are trapped in these radiation belts. Main reason behind these trapping (Van Allen Radiation belt) is the difference between rotational and magnetic axis of the earth [4]

Earth acts as a magnetic dipole and the magnetosphere field lines of the earth trap the charged particles. The field is not uniform around the earth. Geological interferences, tilt in the magnetic axis cause the local distortion in the field and that's how the belts are formed. The inner belt is 1,000KM to 6,000KM and the outer belt is 20,000KM to 40,000KM from surface of the earth. South Atlantic Anomaly (SAA), which extend upto 200KM from Earth's surface (above Brazil) is a specific distortion caused by low magnetic field.

[3]Triple Modular Redundency, error correcting codes, node splitting, dual interlock cell
[4]enclosed layout transistor, guard ring, differential charge cancellation

3.2.2 Galactic Cosmic Rays

Galactic cosmic rays are uninterrupted, low-flux component of space radiations, coming from out of the solar system but within the galaxy. Most of the elements of periodic table are found in cosmic rays as heavy ion particles. Heavy ions, alpha particles and protons of several GeV energy, are part of the cosmic rays.

3.2.3 Solar Flare

Solar atmosphere releases built up magnetic energy in the burst mode, known as solar flare. Solar material is accelerated to high velocity by these solar flares. Low atomic weight solar material radiation with low energy is dominant during solar flare. It can continue up to few hour. The protons, electrons and alphas are emitted in smaller quantity by the sun in bursts during solar storms. It consists of radiations across entire electromagnetic spectrum[5]. The flux, besides being intermittent, vary with the solar cycle.

3.3 Radiation Effects

Radiation effects are characterized as; single–event–effects and cumulative (accumulation) effects, as shown in Figure 3.1 [57]. When ionizing radiation travel through semiconductor material, it will lose energy by means of scattering and different interactions with lattice. Ionization and atomic displacement are the two main interactions, energy particles have with semiconductor lattice. These interactions bring degradation in the performance of a device, over a long period of time.

Striking location and intensity of radiation will determine the level of damage in electronic parts. The effect may be destructive or non-destructive. The non-destructive effects do not damage the device and are termed as 'soft error', while destructive effects which cause permanent damage to integrated circuits is termed as 'hard error'.

[5]From radio waves to X-rays and Gamma rays

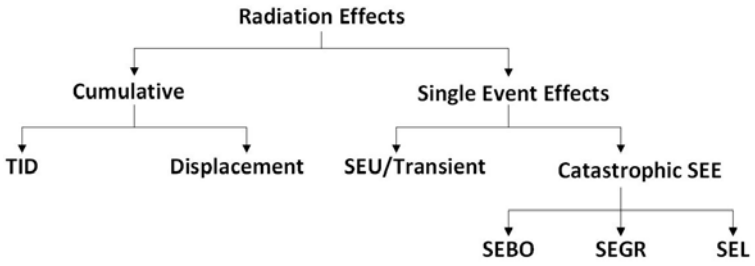


Figure 3.1: Radiation Effects

Cumulative effect:

Displacement damage and total-ionizing-dose (TID) both are cumulative [6] effects. Device parameter tend to change because of these long-term effects.

3.3.1 Displacement Effects:

When an atom in crystal lattice is displaced to another location, it is known as displacement effect. Over a long period of time, these cumulative damages are introduced in semiconductor structure by energy particles. If atoms are moved, a vacancy will be created at that position. These effects are unstable with thermal cycling [5].

3.3.2 Total Ionizing Dose

When radiations strike, they generate electron-hole pairs in bulk as well as in gate oxide layer of the semiconductor. Inside the bulk, free charge, made of electron hole pairs are drifted by potential difference making a current spike. But the charge inside oxide layer does not move quickly. Because of higher mobility of electrons they move toward positive potential (gate for NMOS), while holes do not move much because of their lower mobility. Over a period of time accumulation of holes are inevitable inside oxide layer. Severe degradations are observed in BJT and MOS devices because of the hole trapping inside oxide layer [8],[10].

[6] long-term

Threshold Voltage Shift: When holes are trapped in NMOS gate oxide, they will act as if some potential is applied on the gate terminal and will try to invert the channel in MOSFET. Now its easy to turn on the NMOS device as inversion is already there nad its external threshold voltage is now reduced. This effective potential on gate will be permanent and will grow with time and ionization, making NMOS 'on' without any external gate voltage. In similar way, the PMOS threshold will become higher and it will be difficult to turn it on.

Sub-threshold Slope and leakage: As holes trapped inside oxide layer will change the threshold voltage of the device and hence the sub-threshold characteristic will also change and leakage will either increase (NMOS) or decrease (PMOS).

Transconductance: The transconductance (gain) of the transistor depend upon the drain–current. When threshold voltage is reduced, the drain–current is increased and hence the transconductance is also increased.

Breakdown Voltage: When holes trapped in gate oxide act as if potential is applied on the gate terminal, the maximum voltage which can be applied externally, will change. In this process the breakdown voltage will decrease/increase for NMOS/PMOS.

Noise: Flicker or 1/f noise in MOS transistor is sensitive to the presence of charge–defects near the oxide–silicon interface. In thin MOS oxide layers, additional noise induced by exposure to radiation is correlated with the amount of charge trapped in oxide, generated during irradiation.

Speed: Because of shift in threshold voltage, NMOS becomes faster and PMOS becomes slower. In a circuit how NMOS and PMOS are arranged will determine the overall speed of that circuit.

Functional Failure:

Because of shift in threshold voltage, when NMOS becomes permanent 'on' and PMOS becomes permanent 'off' there may be functional failure. A continuous low or high logic level will appear at output depending on circuit configuration.

ELDRS:

Enhanced Low Dose Rate Sensitivity (ELDRS) is shown by mixed signal

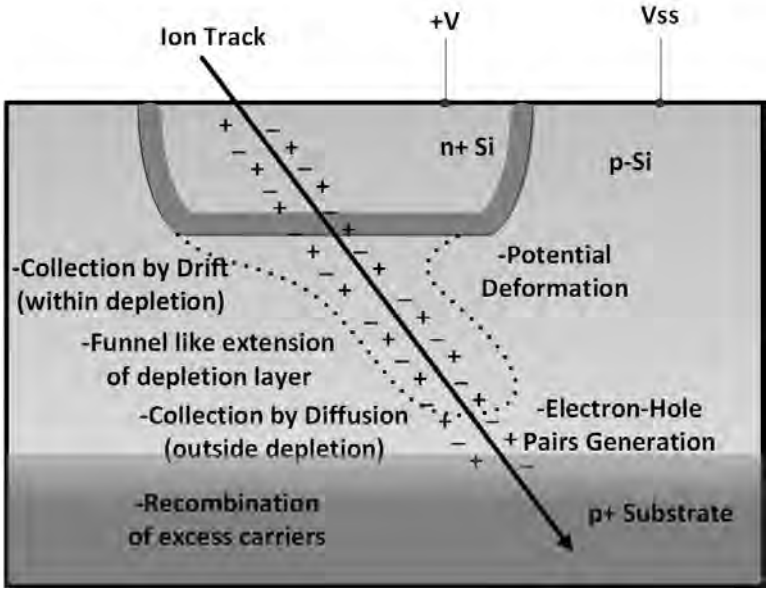


Figure 3.2: Charge collection on a node due to an incident ionized particle

devices utilizing bipolar minority carrier elements. There is no method for predicting susceptibility to ELDRS or simulating the low dose rate effects. The dose rate to test ELDRS, may be as low as 10mrad(Si)/s.

3.3.3 Single Event Effects (SEE)

Heavy ion or proton of high energy can create the single event effects, or SEE. When an incident particle passes through a circuit substrate, the charge is generated in the form of holes and electrons. They drift toward the node of opposite polarity, as shown in Figure 3.2. SEE arecan be of two types one is 'soft error' and another is 'catastrophic'.

Soft–error occur when the ionized charge at the node exceed the critical charge threshold ($Q_{crit} = C_{node}.V_{node}$) of that node. Single event transients (SET) and single event upsets (SEU) are two types of SEE soft errors. SEUs are caused by direct ion strike, inside a latch storage element, while SETs are caused by transient, temporary voltage shifts from preceding logic. SEU occur when logic level at the output of a storage element is changed by ionized charge. It is a temporary effect and non-destructive. It can be corrected by

reset or by reloading the affected bit.

The catastrophic type of SEE can not be corrected and may damage the device [10]. Unlike soft errors, hard (catastrophic) errors created by SEEs like single event gate rupture (SEGR), single event burn-out (SEBO), single event latchup (SEL) can cause unrecoverable failures in CMOS circuitry.

Single-Event Transient (SET): The source of SETs are caused by ionizing particles, striking in combinational logic area. It appears in the form of a pulse.The pulse returns to its proper state once the circuitry driving the affected node removes the collected charge. It is a soft error and temporary in the nature.

Single-Event Upsets (SEU):

Particles striking on an integrated circuit may cause SEU if the charge collected in the substrate exceed the critical charge threshold of that node. Any voltage shifts may potentially be restored to their original value by circuitry driving incident nodes. However in some situations, most notably storage nodes, the charge will not be absorbed and an upset will occur. As mentioned earlier, collected charge affects nodes at or near the place of strike. It may cause SEUs in storage cell, memory or latch. SEU occur when logic level at the output of a storage element is changed by ionized charge. It is temporary in the effect and non-destructive. It can be corrected by reset or by reloading the affected bit.

When ions strike an integrated circuit, charge is deposited as the particle travels through the substrate. The particles stopping power is measured in energy loss per unit path length (MeV-cm^2/mg) which is known as linear energy transfer (LET).

Single-Event Latchup (SEL):

Single event latchup can have catastrophic effect on device, as it can be there for a long time and can be destructive in the nature. Parasitic resistor and BJT in CMOS technology are the main reasons behind single event latchup. Bulk CMOS structure contains parasitic vertical and lateral bipolar pnp and npn transistors which forms pnpn thyristor as shown in Figure 3.3 [57].

When current spike created by ionized electron hole pair, is more than

a certain level, the thyrister will turn on and a low resistance path will be there between supply and ground pins. This low resistance path can create large currents between VDD and VSS. This can lead to local heating and even burnout of the device, and there can be complete loss of the circuit functionality.

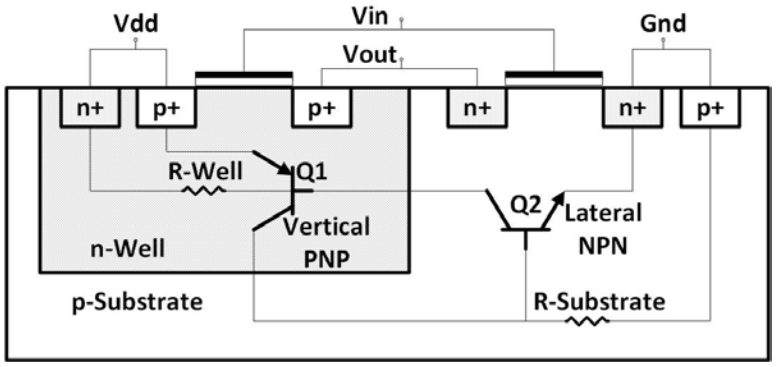


Figure 3.3: Parasitic pnpn thyristor structure

Single-event snapback: Avalanche multiplication of the charge carriers will be there when device is conducting high current and particles strike near drain. It will further induce large currents and device will be open permanently.

Single-event induced burnout (SEB): Because of particle hit large current flows through source junction making it forward biased. A single event burnout may take place during that scenario.

Single-Event Gate Rupture (SEGR): If the gate is connected to high voltage input and at the same time if a heavy ion hits the gate region in MOSFETs, gate oxide breakdown may happen known as single event gate rupture.

3.4 Radiation Mitigation Techniques

Radiation hardening can be achieved by either process or by design or by both [57]. Mitigation techniques, based on design is called 'radiation-hardening-by-design' (RHBD) and based on process is called 'radiation-hardening-by-

process' (RHBP). Different process steps, design techniques and their mitigation capabilities are shown in Table 3.1[57]

Table 3.1: Radiation mitigation techniques

Mitigation Techniques	**TID**	**SEL**	**SET**	**SEU**
Epitaxial layers (Process)		√		
Silicon on insulator (Process)		√	√	√
Shallo Trench Isolation (Process)	√			
Triple Well (Process)		√	√	√
TMR (Architecture Design)			√	√
Encoding (Architecture Design)			√	√
DICE (Circuit Design)			√	√
Edge-Less-Transistor (Layout Design)	√		√	√
Guard Ring (Layout Design)		√		
Differential Charge Cancellation (Layout Design)			√	√

3.4.1 Radiation Hardening By Process (RHBP)

Through specific foundries, which are having special/modified processes[7], the radiation hardening by process is achieved. Radiation hardening by process is done by different ways like use of specific materials, optimization of deposition processes for insulators, modifications of doping profiles in devices and substrates, etc.

SEE and TID are main effects which are dealt with RHBP.

- TID is associated to charge deposition in insulators (*e.g.* gate oxide and field oxide), thus degrading their properties. Because of lower mobility of holes compared to electrons, the net charge trapped in oxide is positive. Now there will be higher leakage current either intra-device (within a transistor) or inter-device (between two adjacent transistors). If doping level and insulator properties are modified near active region, TID can be improved. A technique devoted to mitigate TID concern is Shallow Trench Isolation oxide [58].

[7]Like Silicon-On-Insulator or Silicon-On-Sapphire, epitaxial layer

- For mitigation of SEEs, which are instantaneous errors, different type of substrate/material is used like Silicon On Sapphire (SOS) or Silicon On Insulator (SOI), silicon with epitaxial layers, so that effective active area where charge can develop is reduced.

Epitaxial layers The principle is to get a thin lightly-doped epitaxial layer over a low-resistivity or highly-doped substrate as shown in Figure 3.4. The gain of the parasitic transistor and the value of parasitic resistor both are reduced by low resistivity substrate. The ionized charge can be collected by low resistivity substrate. All these factors help in hardening against latch-up [11], [12].

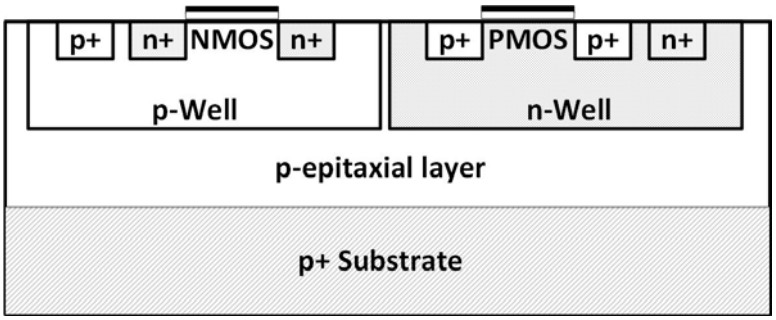


Figure 3.4: Epitaxial Layer

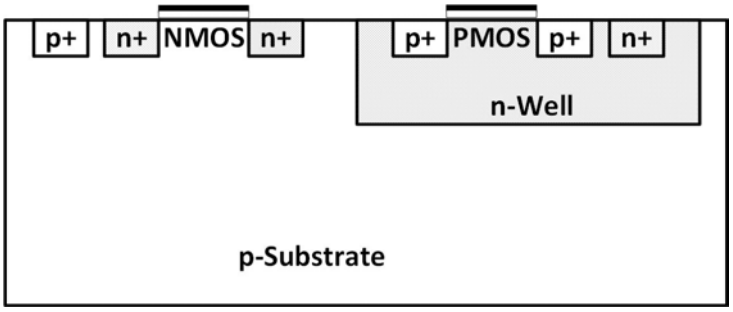
Triple Well

NMOS and PMOS both are used in a CMOS process. To fabricate both types of MOSFET, there can be single-well, dual-well or triple-well in a CMOS process, as shown in Figure 3.5 [15, 57].

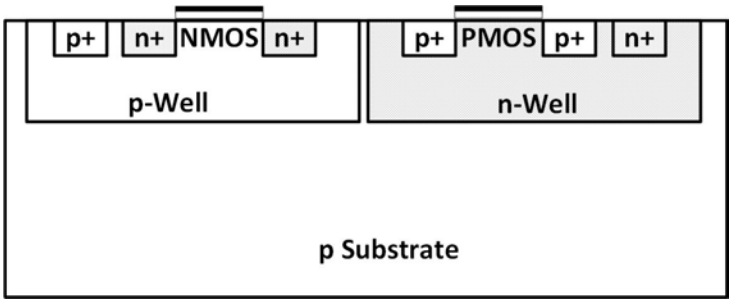
- For a single well p-type substrate process, there will be an n-well to make PMOS device as shown in Figure 3.5(a). This process is less expensive to produce circuits, however, at the cost of lower-performance chips, because the devices characteristics cannot be optimized. Moreover, it requires a heavily doped substrate, thus increasing the probability of having SEL.

- Dual[8] well process provide well for both type of devices on a lightly

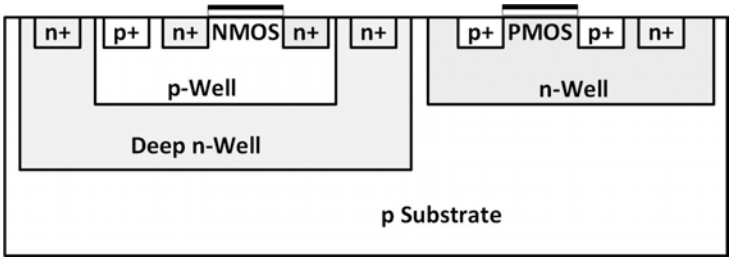
[8]also known as twin-well process



(a) Single Well



(b) Dual Well



(c) Triple Well

Figure 3.5: Different type of well technologies a)Single, b)Dual, c)Triple

doped substrate. There will be n-well for PMOS and p-well for NMOS device as shown in Figure 3.5(b). As both the devices are placed in separate wells, it is possible to optimize both the devices separately. Both the devices can be tuned independently for channel transconductance, body effect, threshold voltage etc. A high resistivity zone is provided by lightly doped substrate which reduces the risk of latchup compared to the single-well process.

- In a dual well process, at least one well will be of the same type as of

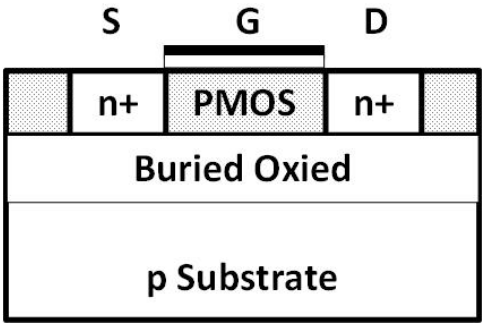


Figure 3.6: Silicon on Insulator structure

the substrate (it will be extension of substrate) and hence the well will not be isolated from substrate. As shown in Figure 3.5(b), the p-well is extension of p-type substrate. Triple well technology provides isolation from the substrate for both the wells by means of reverse biased pn-junction. In a p-type substrate, n-well is created for PMOS devices and p-well is created for NMOS devices. Here, to separate the p-well from p-type substrate, the p-well is created in side a deep n-well which is the third well as shown in Figure 3.5(c). In this way substrate collection is reduced for both devices by reverse biased isolation.

Silicon On Insulator In bulk CMOS process, carrier transportation take place in only the top region of bulk, the remaining inactive-part[9] of the silicon provide the mechanical support. This inactive region contribute in leakage currents. In SOI process, transistor are built on a thin layer of silicon, which is deposited on insulating layer of silicon dioxide (SiO_2) as shown in Figure 3.6 [57]. SOI inherently eliminates latchup, as parasitic thyristor effect is not there in oxide isolated wells [13]. Because of small deposited silicon layer, charge collection volume is very less in SOI compared to bulk CMOS, and hence it is less susceptible to SET and SEU. Sapphire[10] (Al_2O_3) is another type of insulator where it works as substrate and a thin film of silicon is deposited on it. There will be hetero-junction between Silicon and Sapphire as both have dissimilar crystalline structures compared

[9]Which is around 99% of the bulk
[10]In Silicon On Sapphire (SOS) Process

to Silicon and Silicon-dioxide junction.

3.4.2 Radiation Hardening By Design (RHBD)

In contrast to the RHBP, the RHBD technique dose not need any process modification and can be implemented on standard CMOS fabrication process. The RHBD mitigation techniques can be implemented at different levels like circuit (or architecture) level and at layout level.

Architecture level- This technique is specific to the type of circuit like analog/mixed signal, digital. Some techniques under this category are Dual Interlock CEll (DICE), Error Correcting Codes (ECC), triple-modular-redundancy (TMR), Node splitting, etc..

Layout level- In this technique layout and placement of transistor is done in such a way that it become less sensitive to the radiation. Few of the techniques are guard rings, edgeless transistor, differential charge cancellation (DCC), etc.

Triple-Modular-Redundancy (TMR)

This is an architecture–level method of RHBD in which the design is triplicated and thats how two redundant circuits are introduced. As shown in Figure 3.7 the state machine is instantiated three times, with one voter. An SEU can corrupt the part of one of the blocks, but majority voting restores the correct state. It requires three times area for implementation [80].

Error Correcting Codes (ECC)

This is an architecture–level technique of RHBD, where redundant information (bits) and encoding-decoding mechanism is implemented. Forward Error Corrections (FEC) or Error-Correcting Codes (ECC) have capability to detect and/or correct errors in bits. This is achieved if some redundant bits or parity bits are added to the original data bits. While writing in to memory, data is passed through an encoder, which introduces some redundant bits (parity). The validity of original data is checked while reading, using these

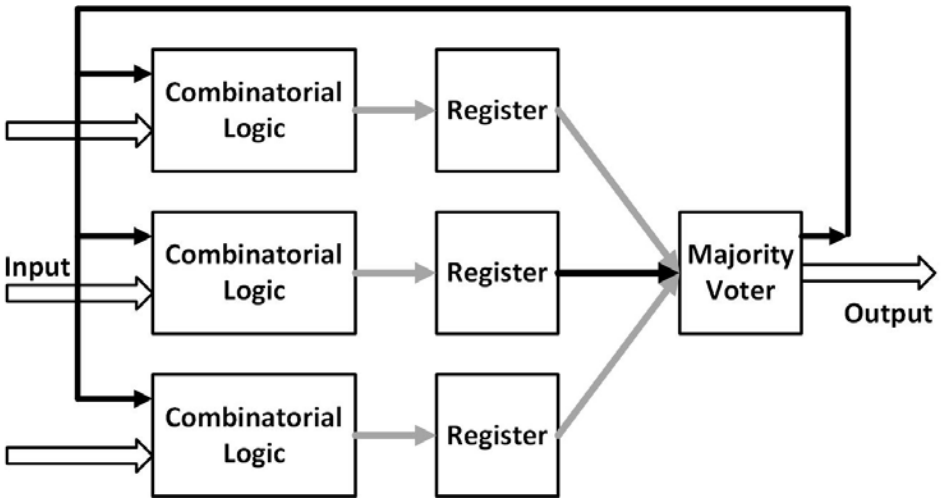


Figure 3.7: The concept of triple-modular-redundancy

extra redundant bits. While reading back, the data is passed through a decoder which determines if there is any bit flip and if there is any, the decoder can correct the error as shown in Figure 3.8. Most commonly used error correcting codes in space and aeronautic applications are Parity checking, Cyclic Redundancy Check, Hamming, Reed-Solomon, and Turbo codes [24]. Different error correcting codes have different capability to detect and/or correct the error in data. Error correcting codes are of two types: convolution codes and block codes. In data-storage applications, block codes are used while in data-transfer applications, convolution codes are used. Block codes can be of two types, either they can only detect the error or they can detect as well

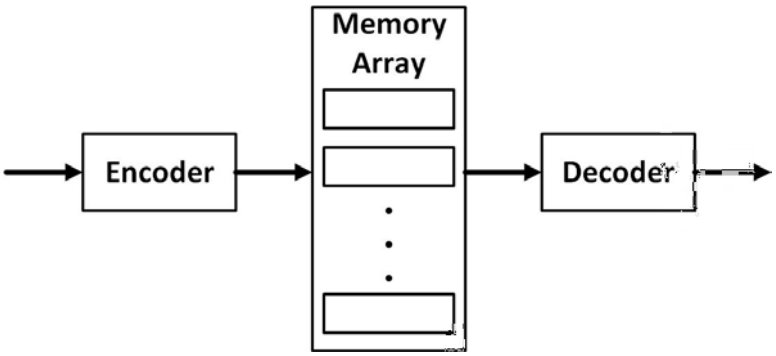


Figure 3.8: Encoding method

as correct the error in the data. The capability of the error correcting codes depend on the number of redundant bits. All error correcting codes have disadvantage of time-overhead and area-overhead.

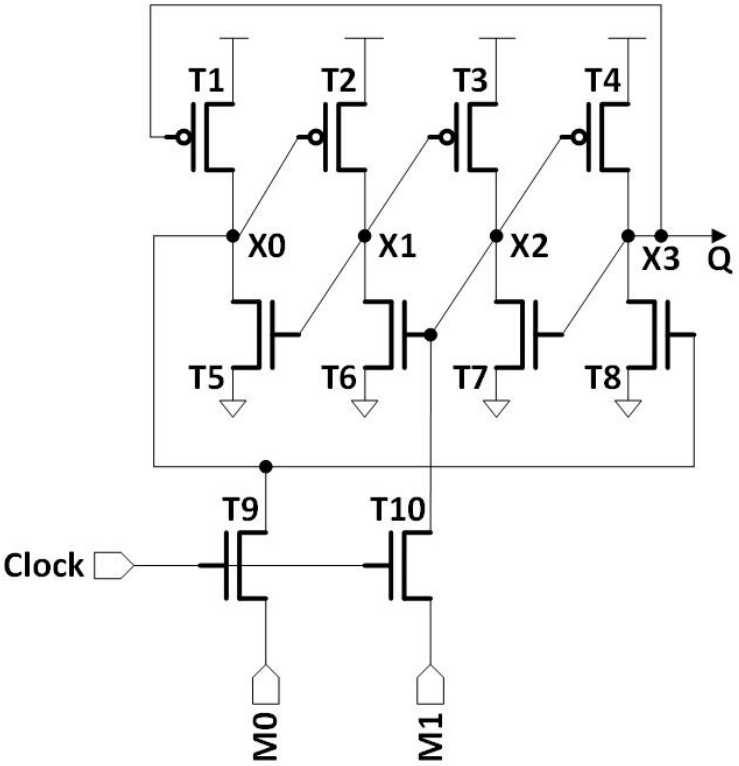


Figure 3.9: Dual Interlock CEll (DICE) structure

Dual Interlock CEll (DICE)

It is a circuit level technique of RHBD, where a different transistor configuration is used rather than conventional one. Dual Interlock ensures SEU protection against radiation hit on one node. Local redundancy, or interlocking, utilizes feedback storage nodes to mitigate SEUs. The effect of parameter variations and transistor size ratios on DICE architecture is very less. There are ten MOSFETs used in a DICE based latch as shown in Figure 3.9 [21]. The feedback paths in this design insure that single node upsets are quickly corrected. At least two storage nodes in the latch must be driven by inputs in

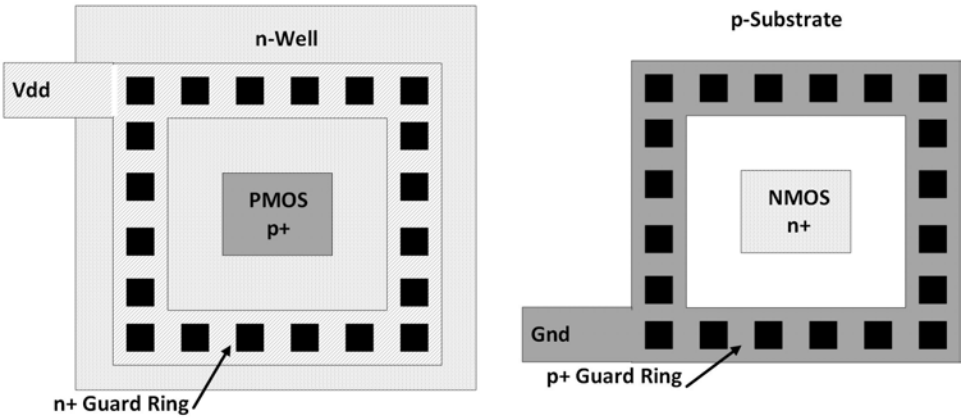


Figure 3.10: Guard ring structure

order for the latch to write properly. This combats the interlocking feedback paths from fighting latch input signals. All four storage nodes can be written at once to improve write speed. Implementing DICE latches in layout provides a compact, low power design. Generally, node X0 is at the same state as node X2. Similarly, node X1 is at the same state as node X3. The output Q, which corresponds to node X3, is generally the opposite logic state that is stored on nodes X0 and X1. In order to achieve radiation hardening of the DICE latch, the nodes X0-X3 must be physically separated from each other to an extent that will prevent any two of the nodes X0-X3 from being hit by a single radiation particle. As a result only one of the nodes X0-X3, is struck by a radiation particle.

Guard Ring

In the CMOS process if parasitic thyristor is formed as shown in Figure 3.3, it may cause latchup. The thyristor effect can be minimized by guard rings which will reduce parasitic resistance of well (R_{Well}) and substrate ($R_{Substrate}$). Guard ring around MOSFETs have been found to be very effective against single-event-transients (SETs) [20]. Guard ring structure for PMOS and NMOS are shown in Figure 3.10. In this layout method parallel contacts are placed between source-substrate/well (for NMOS), and between drain- substrate/well (for PMOS). This will reduce source-well contact resis-

tance and hence will reduce the parasitic resistance. Guard ring structure helps in removing the ionized charge from drain/source area to VDD/VSS through low resistance path. So that parasitic resistor is drastically reduced and the voltage developed across these resistors will not be enough to trigger the thyristor [18].

Edge- Less Transistor

To reduce the impact of radiation, Enclosed-Layout-Transistor or Edge-Less-Transistor (ELT) is used in place of standard rectangle layout. As thick field oxide (STI), is situated nearby gate oxide and has larger tendency to capture free charge, it affects overall control on transistor. In Edge-Less-Transistor, the gate is completely surrounded by source or drain, no field oxide is available near the gateas shown in Figure 3.11. This technique has advantage of no birds–beak leakage effect on device, which reduces TID effect and it also prevents SEU [16]. It has complex model of transistor behavior and it also consume large area. In this technique there is a limitation on aspect–ratio, which is available for design, as any random aspect ratio can not be implemented. Because of its complex structure it is difficult to model it and lot of work has been done on that [17].

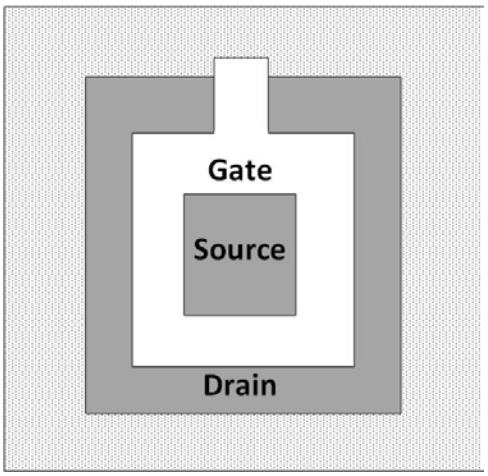


Figure 3.11: Edge-Less (Enclosed-Layout) Transistor

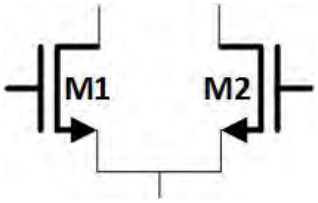
Differential charge cancellation (DCC)

Another layout design technique of radiation hardening is Differential Charge Cancellation (DCC). The charge, which is responsible for single event transient in differential circuits, is shared and converted in to common mode signal, which in turn rejected by constant tail current of differential circuit. The single ended error signal is converted in to common mode signal by a simple change in layout. Generally, source terminals of differential pair transistors are kept nearby, while in this technique drain terminals of differential pair is kept close, so that any transient on drain nodes become common to both the transistors as shown in Figure 3.12 for a differential pair M1-M2 [25]. Keeping source terminals of differential pair close in layout is not useful as they are anyhow connected and any transient at source node is already a common mode signal. This layout technique does not have any area or matching penalty compared to common-centroid layout. Radiation sensitive area is drastically reduced if this layout technique is used and it is more effective in lower technology nodes.

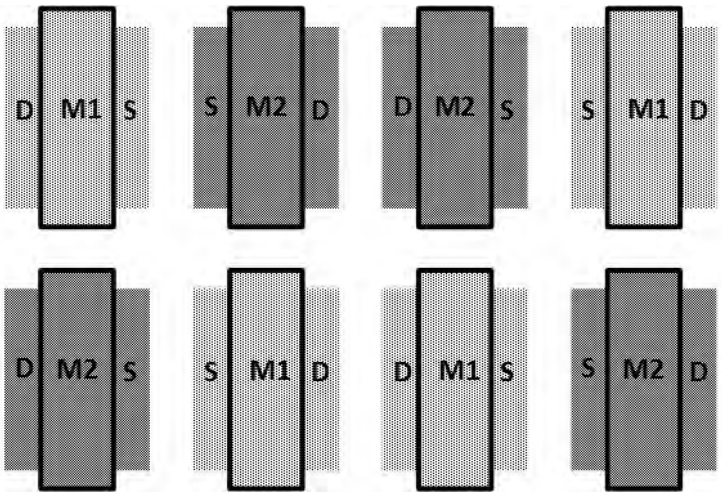
Node Splitting Technique

Continuous-time analog/ mixed signal circuits and switched-capacitor circuits can be hardened against single-event-effects, by creating parallel signal paths known as 'node splitting' [26]. It is a radiation hardening by design technique at circuit/architecture level. The circuit is split/peeled in such a way that internal nodes are parallel sub-circuits paths which are shorted at output and input node as shown in Figure 3.13 [59]. Electrical performance of the original un-peeled circuit is maintained at peeled level by proper transistor sizing of sub-circuits. When ionizing radiation strikes and tries to upset one sub-circuit, while other sub-circuits will behave normally and will nullify the effect of transient at output. Hardening via node splitting technique can be implemented in two ways: peeling only sensitive nodes (smart peeling) or peeling all the internal nodes[11].

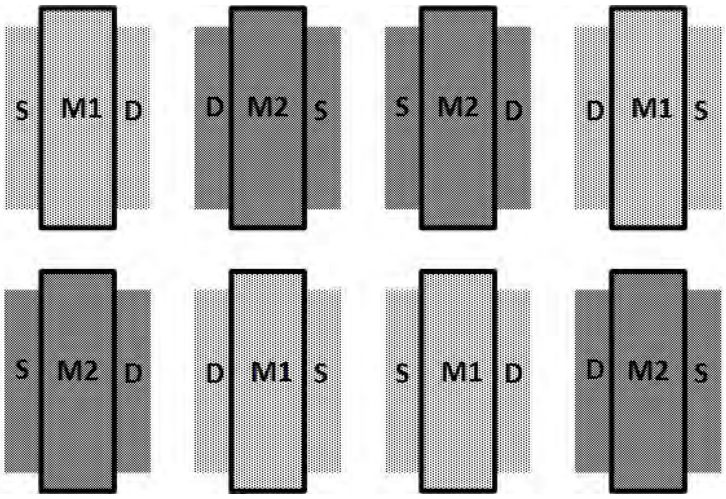
[11]Massively Multiple Peeled Layout (MMPL)



(a) Differential pair



(b) Common-centroid layout



(c) DCC layout

Figure 3.12: (a)Differential pair (b) Standard common-centroid layout of differential input stage (c) DCC layout

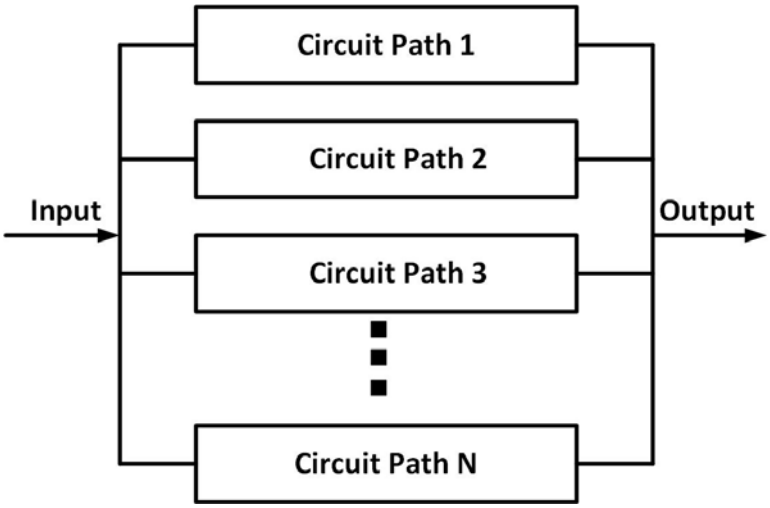


Figure 3.13: Node splitting concept

Chapter 4

Addressable Synchronous Asynchronous Differential Receiver Design in 0.18μm CMOS

In this Chapter, the design of a mixed signal Addressable Synchronous-asynchronous Differential Receiver (ASDR) ASIC with 0.18μm CMOS process is discussed. The block diagram of ASDR ASIC is shown in Figure 4.1. The analog module consists of three RS422 differential receivers with a single RS422 differential transmitter (driver), a 3.3V-to-1.8V Linear Voltage Regulator (LVR), a Power On Reset (POR) and a Clock Generator (CG) circuit. The serial-to-parallel conversion logic with multiple modes is part of the digital block. ASDR receives serial data as differential (RS422) signals and provides 16-bit parallel output. It can handle both synchronous and asynchronous serial data as shown in Figure 4.2 [60],[61]. ASDR has three synchronous modes and one asynchronous (UART) mode. It takes three differential input signals (data, clock, strobe) during synchronous communication or one differential input signal (data) during asynchronous communication and converts these serial data in to 16 bit parallel data. The auto baud lock feature is implemented in the design for asynchronous mode. The

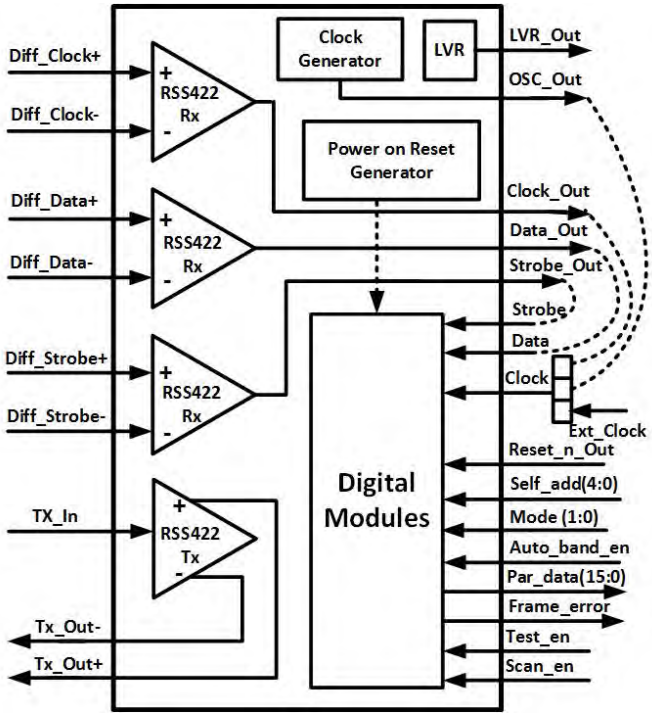
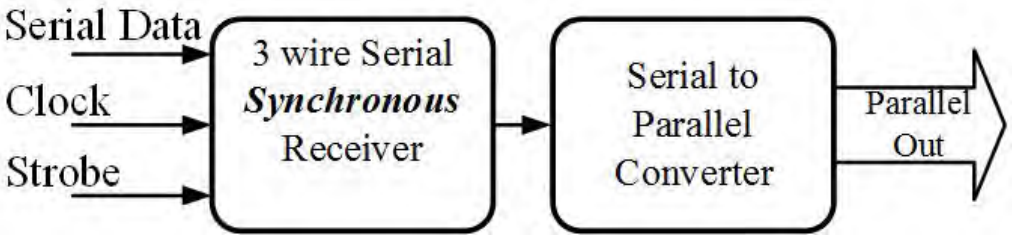


Figure 4.1: Block diagram of Addressable Synchronous-asynchronous Differential Receiver (ASDR) ASIC

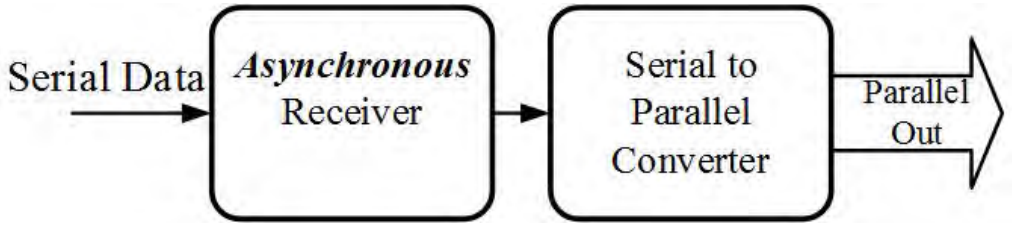
design has 5 bit self-address feature, which is useful when devices are used in multi-drop configuration . Additionally it supports using all the analog and digital modules separately. There are three options for providing clock to digital block either via a differential-receiver or from an on-chip clock-generator or from an external source.

4.1 Analog Modules

The analog modules of ASDR consist of a differential receiver and a transmitter, POR circuit, a clock generator and a linear voltage regulator.



(a) Synchronous (Data, Clock, Strobe) Receiver



(b) Asynchronous Receiver

Figure 4.2: Block diagram of (a)Synchronous receiver; (b)Asynchronous receiver.

4.1.1 RS422 Differential Receiver

The RS422 differential receiver circuit receives the differential signal and converts into single ended TTL/CMOS level signal. The standard differential receiver architecture is based on two–stage amplifier [62]. The first stage (differential-amplifier) provides amplification to low level differential input and converts into single ended signal. As shown in Figure 4.3, transistors M2 and M4 are in parallel with input pair M1 and M3 respectively. Transistors M2 and M4 are native MOSFETS with near-zero threshold-voltage [63, 64]. These native MOSFETS increase the input Common Mode (CM) range of the differential receiver. The low threshold voltage (V_{th2}, V_{th4}) of M2 and M4, help in reducing the voltage headroom requirement as shown in equation (1) and (2). The high (maximum) value of input common mode voltage CM_{High} is given by:

$$CM_{High} = (V_{dd} - V_{GS5} + V_{th1}) \tag{4.1}$$

and the low (minimum) value of input common mode voltage CM_{Low} is given by:

$$CM_{Low} = V_{OV7} + V_{GS2} = V_{OV7} + V_{OV2} + V_{th1,2} \tag{4.2}$$

Where $V_{OVn}(\approx 0.1V)$, V_{GSn} and V_{thn} are overdrive, gate-to-source and threshold voltage of MOSFET M_n respectively [65]. The V_{th2} is threshold of native NMOS ($\approx 0V$) and V_{th1} is threshold of standard NMOS ($\approx 0.4V$). Here combination of native and standard threshold ($V_{th1,2}$) have been used to reduce CM_{Low} and hence increase the input-common-mode-range.

The gain of first stage (A_{V1}) is given by:

$$A_{V1} = g_{m3}(r_{o3}||r_{o4}||r_{o6}) = \frac{2(I_3 + I_4)}{V_{OV3}(I_3 + I_4)(\lambda_n + \lambda_p)} \tag{4.3}$$

where g_{mn}, r_{on} and I_n are transconductance, output-resistance and drain current of M_n MOSFET. The channel length modulation coefficient of N-MOSFET and P-MOSFET is λ_n and λ_p respectively. The drain current I_3 is :

$$I_3 = \frac{\mu_n C_{ox} W}{2L}(V_{GS3} - V_{th3})^2 = \frac{\mu_n C_{ox} W}{2L}(V_{OV3})^2 \tag{4.4}$$

where μ_n is mobility of electrons, C_{ox} is gate-oxide capacitance and W and L are width and length of MOSFET respectively.

$$\frac{W}{L} = \frac{2I_3}{\mu_n C_{ox} V_{OV3}^2} \tag{4.5}$$

The second stage (common-source) amplifier is implemented with transistors M8 and M9. The gain of the second stage (A_{V2}) is given by:

$$A_{V2} = g_{m8}(r_{o8}||r_{o9}) = \frac{2I_8}{V_{OV8} I_8 (\lambda_n + \lambda_p)} \tag{4.6}$$

Simulation results of differential–receiver are shown in Figure 4.4, where In1 and In2 are inputs. The inputs are applied differentially with a difference

of ±200mV and varied across complete common mode input range (CMIR) from 0.5V to 2.8V in a sinusoidal manner. It is observed and shown in Figure 4.4, that differential receiver could resolve ±200mV difference across CMIR for different PVT corners.

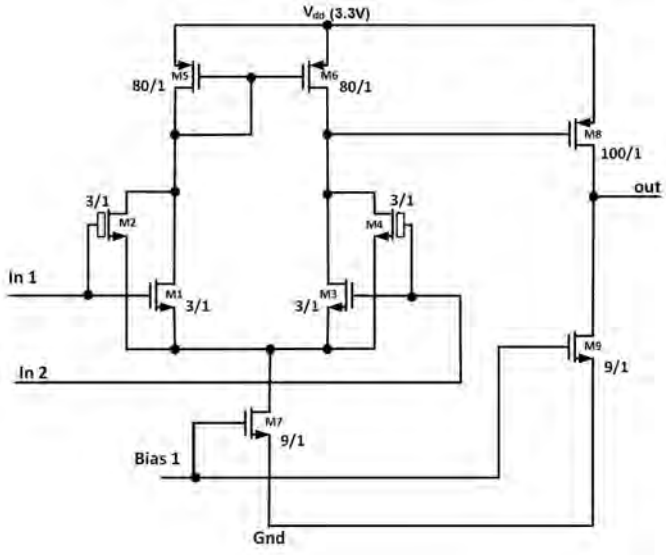


Figure 4.3: Transistor level implementation of differential receiver, two native transistors M2 and M4 are shown with box shaped Gate terminal

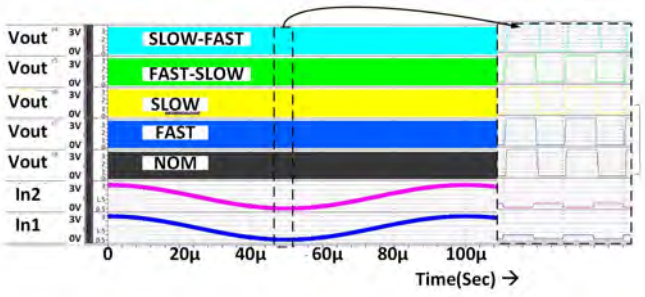


Figure 4.4: Simulation Results of Differential Receiver

4.1.2 RS422 Differential Transmitter (Driver)

The differential transmitter converts a TTL/CMOS level, single ended signal into a differential signal [66]. As shown in Figure 4.5, the transmitter circuit

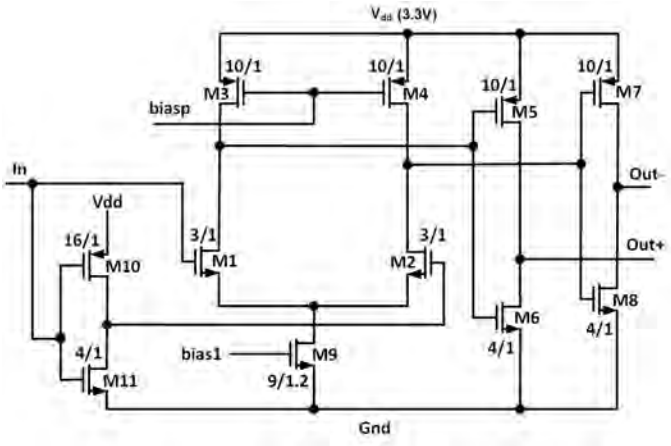


Figure 4.5: Transistor level implementation of Differential Transmitter.

consists of a single end to differential converter (M1,M2), load transistors (M3,M4), buffer stages for positive (M5,M6) and negative (M7,M8) outputs. The buffer stage provides drive to the differential output signals. There is no need to control the output-common-mode (DC) voltage, as receiver input-common-mode range is large enough. Simulation results of differential transmitter for various PVT corners are shown in Figure 4.6. For realistic loading conditions, the differential transmitter is simulated with five sections of Gore cable R-L-C model (equivalent to 5 meter) [67]. The Gore cable model and the RLC values are shown in Figure 4.7. It is observed that level of generated differential signals, is above 2V, which is in accordance with the RS422 standard, under loading conditions. With the inclusion of the transmitter, the ASDR behaves as transceiver for asynchronous serial data. In other words, one ASDR device can transmit asynchronous serial data, while on other end, another ASDR can receive the data.

4.1.3 Power on Reset Generator

The POR circuit is required to bring the digital module to a known state, at power-on condition. The clock-generator should be stable before the POR is de-asserted. Therefore the duration of reset pulse width generated by POR should be more than the settling time of the oscillator. The POR generates

a low level pulse of minimum 40μs duration at power-on and then goes high (to 1.8V). The POR circuit, shown in Figure 4.8 is operating at 1.8V supply and has an AND gate to accommodate the external reset, where R=233KΩ and C=500pF. Simulation results of the circuit for various PVT corners are shown in Figure 4.9. From simulation it is evident that the pulse of 40μs is obtained for the fast corner and will not be less than that for any PVT corner. However to accommodate all the other process corners, a slightly higher pulse duration of 56μs, at typical corner is considered for operating this device.

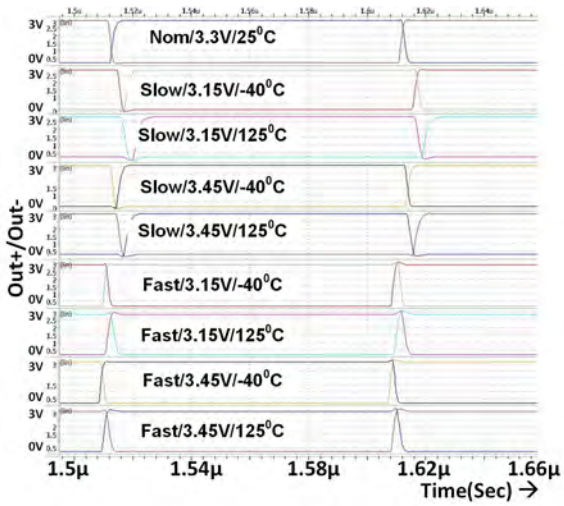


Figure 4.6: Simulation Results of Differential Transmitter

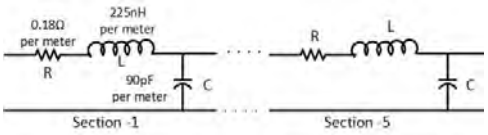


Figure 4.7: Gore Cable model for section of one meter length. Similar 5 sections are cascaded for 5 meter cable

However to accommodate all the other process corners a slightly higher pulse duration of 56μs at typical corner is considered for operating this device.

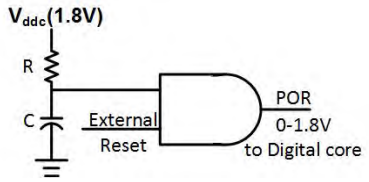


Figure 4.8: Active–low Power–On–Reset generation circuit

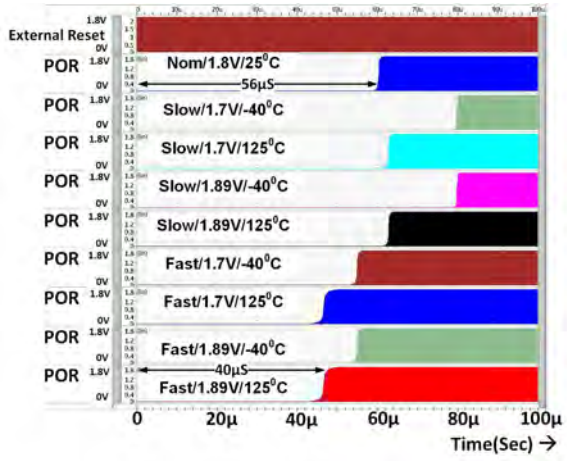


Figure 4.9: Simulation Results of Power-on-Reset circuit for different process corners

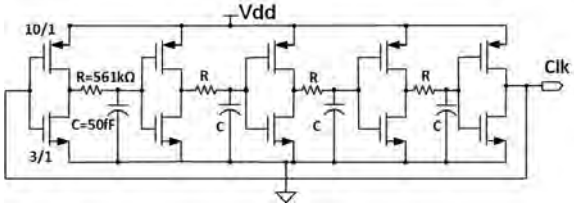


Figure 4.10: Clock-generator consisting 5-inverter stages and 4-RC sections.

4.1.4 Clock Generator

As shown in Figure 4.10 , the clock-generator is based on RC-ring oscillator [68]. It is designed to generate a clock of 4 MHz with 49-51 % duty cycle. In order to keep the temperature variations at minimum, only 5-stages of inverters are used and the remaining delay is obtained from the RC stages [69]. As without these RC delays, the number of inverter stages would go up to more than 500. Tf the temperature increases by 1^0C, the threshold voltage

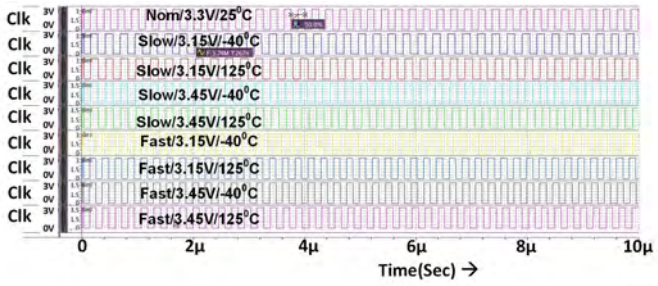


Figure 4.11: Simulation Results of RC-ring Oscillator.

of the MOSFET will decrease by 2mV, and will cause frequency variation in the generated clock. So it is required to limit the number of inverter stages (*i.e.* number of MOSFETs) to limit the effect of the temperature variations. R and C chosen for this design, have very low temperature coefficients. The simulation results of Oscillator for various PVT corners are shown in Figure 4.11. The effect of temperature on oscillator is discussed in results section.

4.1.5 3.3V to 1.8V Linear Voltage Regulator (LVR)

The LVR is a hard IP developed in home organization and it is used to generate 1.8V from a 3.3V supply. The 1.8V supply is required for digital core and the IOs. Block diagram of LVR is shown in Figure 4.12. The internal reference generator provides a reference-voltage V_R which is independent of supply and temperature variations. The error amplifier compares V_R with the

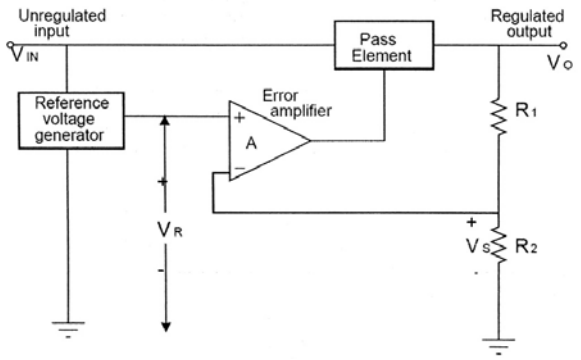


Figure 4.12: Block diagram of Linear Voltage Regulator

sampled (and the scaled) output voltage V_S and generates corrective signal to regulate the voltage drop across pass element so that V_R=V_S holds true. The scaled voltage is derived from voltage divider, R_1 and R_2. The output voltage is given by:

$$V_o = V_R[1 + \frac{R_1}{R_2}] \tag{4.7}$$

The specifications of LVR are shown in Table 4.1. It occupies large area on the chip as it was originally designed for 150 mA of load current.

4.2 Digital Modules

The digital module of ASDR converts serial (synchronous as well as asynchronous) data into 16-bit parallel output. It has a 24-bit word format, out of which the first 5-bits are assigned to address, 16-bits to data and the remaining 3 bits are reserved. It has four operating modes selectable by two mode pins.

Mode-0(00): Synchronous 24 bit data, strobe of 24 bit

Mode-1(01): Synchronous 24 bit data, strobe width of 1 bit

Mode-2(10): Synchronous 16 bit data and gated clock

Mode-3(11): Asynchronous 8 bit UART

Mode-0 and Mode-1 are synchronous modes and having difference in the type of strobe only. Mode-2 is compatible with serial-peripheral-interface

Table 4.1: LVR Specifications

Sl No.	***Parameter***	***Value***
1	Nominal Output Voltage	1.8V
2	Load regulation	0.31 %
3	Line Regulation	0.3 %/V
4	Output Impedance	212mΩ
5	PSRR (DC),(100KHz)	(67/57), (20/19) dB
6	Dropout Voltage (No load/full load)	0.44/0.35 V
7	Power Efficiency	52%

Table 4.2: I/O table for Digital Module

Name	***Direction***	***Description***
mode(1:0)	Input	2 bit Mode Selection
self_add (4:0)	Input	5 bit Self Address
reset_n_ext	Input	Active Low reset
clk	Input	Serial Clock / Master Clock
ser_data	Input	Serial Synchronous / Asynchronous Data
ser_stb	Input	Strobe
auto_baud_en	Input	Auto Baud-rate Enable Signal
test_en	Input	Test enable signal for Scan Chain testing
par_data (15:0)	Output	16 bit Parallel Output
frm_err	Output	Active High Frame Error Signal

(SPI). The Mode-3 is UART based and can be used in communication with comm/serial port of PC[1]. Block diagram of digital module is shown in Figure 4.13 and I/O description is given in Table 4.2

4.2.1 Mode-0:

This mode will receive 24-bit synchronous data over 3-wire (data, clock, strobe) serial channel and convert into 16-bit parallel output. Out of the 24-bits of serial data, the first 5-bits are self-address, next 3- bits are reserved and last 16 bits are data which is converted into parallel output. This output is updated only if the first 5-bits of serial data (address) are matched with

[1]after converting RS232 into RS422 levels

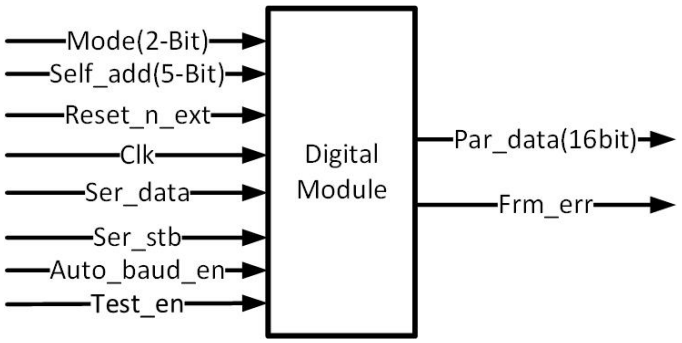


Figure 4.13: Digital Module

self-address input-pins. Shifting in of serial data is done on falling edge of the clock. The most significant bit is shifted in first. The timing-requirement diagram for mode-0 is shown in Figure 4.14(a). The strobe in Mode-0 is active low, encapsulating all 24-bits of serial data.

4.2.2 Mode-1:

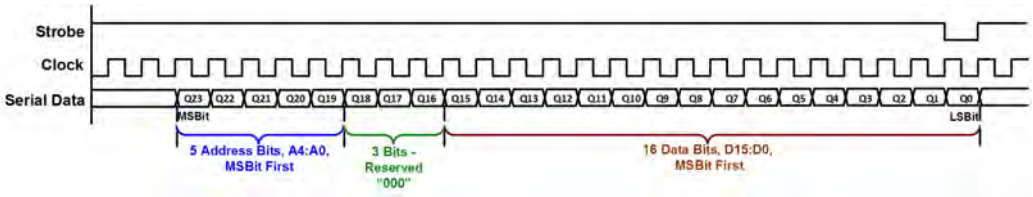
This mode is similar to mode-0 except it requires strobe length of 1-bit at the end of 24-bit data. The strobe is active low for only 24th data bit. The timing-requirement diagram for mode-1 is shown in Figure 4.14(b).

4.2.3 Mode-2:

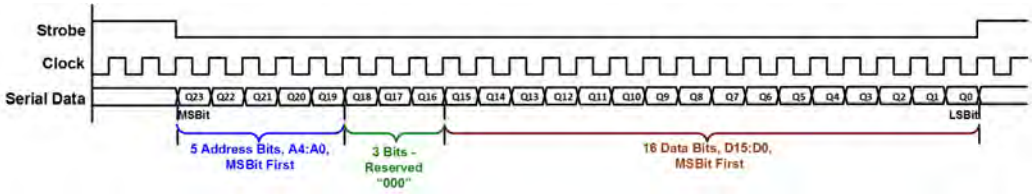
For Mode-2, the 16-bit serial data is transmitted with gated clock along with an active high strobe, which is required at the end of the data. This mode does not require any address bits. The timing-requirement diagram for Mode-2 is shown in Figure 4.14(c).

4.2.4 Mode-3:

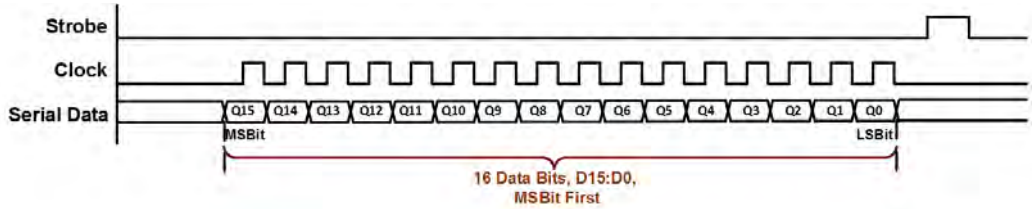
The UART is an asynchronous mode with one start bit, one stop bit and 8-bits of data [70]. It will receive 24-bits and convert into 16-bit parallel output. The parallel data is updated only if 5-bits of address are matched with self-address input pins. In addition, there are two options to select baud-rate, with the help of auto-baud-enable input pin. If auto-baud-enable is 0, then the module will accept the fixed baud-rate of (9600) at 4 MHz clock frequency. If auto-baud-enable is 1, it will accept any baud-rate provided the clock frequency is 16 times higher than the required baud rate. The timing-requirement diagram for Mode-3 is shown in Figure 4.14(d). If position of the stop-bit (which is 9th bit with respect to the start-bit) is not matched, data will be discarded and frame-error (frm_err) flag will be set. Frame-error flag will get reset on next correct reception of 8-bit data.



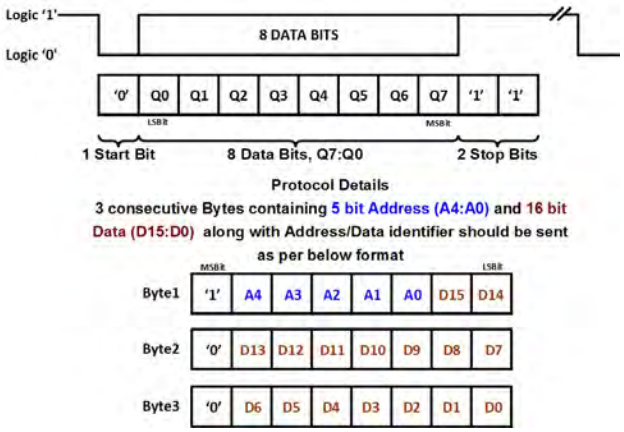
(a) Mode-0



(b) Mode-1



(c) Mode-2



(d) Mode-3

Figure 4.14: Timing-requirement diagram for (a) mode-0, strobe bit at the end; (b)mode-1, strobe is along the complete data length; (c) mode-2, having gated clock and strobe at the end; (d) mode-3, UART (asynchronous) mode.

4.3 Test Results

The ASDR has been fabricated using $0.18\mu m$ CMOS process, the layout is shown in Figure 4.15. The die size is 3.5x3.5mm^2 and the chip is packaged in a 64-pin CQFP. The specifications of the ASIC are given in Table-4.3,4.4. Furthermore, following chip level tests were conducted to ascertain functionality and performance of the device.

4.3.1 Functional Test:

As shown in Figure 4.16, a test-board is designed, consisting ASDR ASIC, standard RS422 Trans-receiver chips and an Oscillator. RS422 of ASDR ASIC was interfaced with standard RS422 chip on the test-board, to test the compatibility with standard device. Actual photograph of test-board is shown in Figure 4.17. A Pattern-Generator is used to generate the multi-

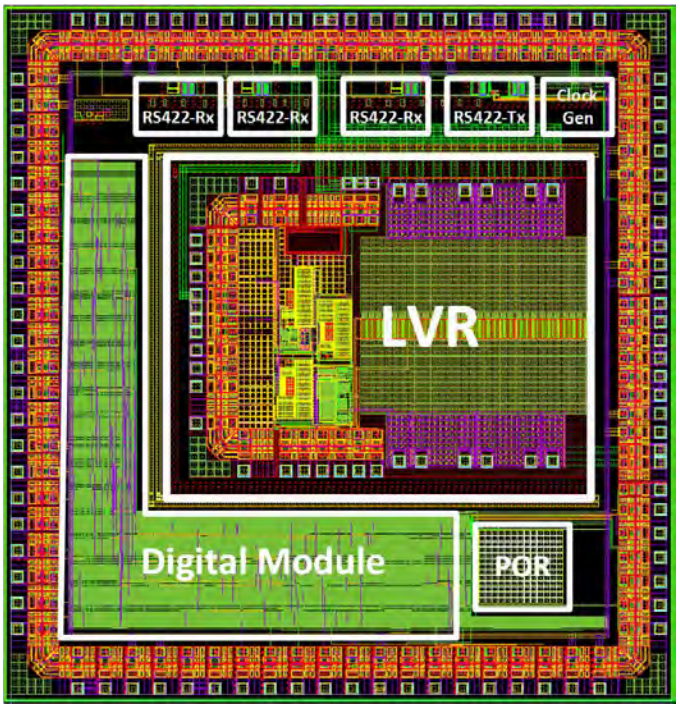


Figure 4.15: Layout of Addressable Synchronous asynchronous Differential Receiver, having die size of 3.5mm x 3.5mm

mode serial data, 3.3V supply is provided by standard power-supply unit and 1.8V supply is taken from the on-chip LVR. Outputs are captured on DSO and Logic-Analyzer. The measured value of CM_{Low} is around 0.4V. From equation 4.2 we observe that $V_{th1,2}$ is around 0.2V which is average of $V_{th1}(\approx 0.4V)$ and $V_{th2}(\approx 0V)$.

The photograph of the laboratory test-setup is shown in Figure 4.18. The functional test of the ASDR ASIC was carried out using Teradyne Ulraflex VLSI tester. A set of VCD test vectors were generated for the test. Three basic tests were performed to check the chip: **(a) Continuity Test:** In this test 100 μA current is forced into input pin and the voltage is measured on that pin. The measured voltage should be equivalent to threshold-voltage of ESD diode (typically around 0.6V). This test is conducted to check the condition of ESD diodes.

(b) Leakage Current Test: In this test the leakage currents (I_{IH} and I_{IL}) are measured and the value should not exceed 100 nA. This test is conducted to check any damage at the input gate-terminal of the transistor.

(c) Static Supply current Test: There are total six types of supplies used in ASDR ASIC and static current is measured at all the supply pins. The measured values of static current are shown in Table-4.5. This test is conducted to check the shorts between supply and ground tracks.

The clock-generator waveform captured on DSO is shown in Figure 4.19.

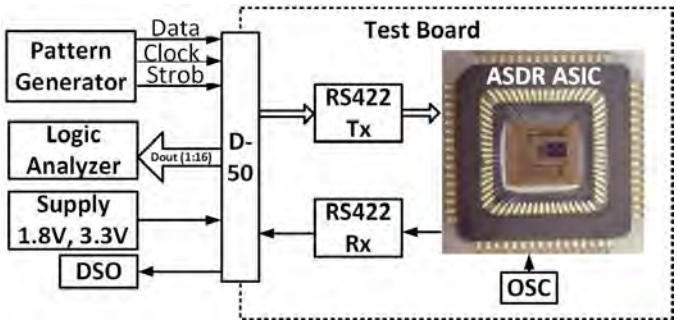


Figure 4.16: Block diagram of functional test-setup, for ASDR ASIC. Test board is shown with ASDR ASIC, RS-422 Tx, RS-422 Rx, Osc along with D-50 pin connector. Standard equipment *i.e.* Pattern generator, Logic analyzer, Supply unit and DSO are interfaced with test board.

Table 4.3: Specifications of ASDR

Parameter	***Specification***
Power Supply	I/O-3.3V, Core -1.8V
Digital Output	16-bit 3.3V CMOS
Analog Inputs	RS422-Differential
Digital Module Speed	50MHz
Digital Gate count	43K
Power Dissipation	130mW
Package	64 pin CQFP
Die Size	3.5mm x 3.5mm

Table 4.4: Specifications of Differential Receiver

Parameter	***Specification***
Power Supply	3.3V
Output Level	0 to 3.3V
Input Sensitivity	-200 to +200 mV
Speed	10 Mbps
Common Mode Input Range	0.4 to 2.8V
Delay	10nS

Table 4.5: Static Supply Current Test

Supply Name	***Measured Values***
Idd (1.8V IO)	29.3185μA
Idd_digital (1.8V Digital Core)	93.3865μA
Iddo (3.3V IO)	1.3442mA
Idd_LVR (3.3V)	7.0143mA
Idd_OSC (3.3V)	762.6112μA
Idd_Tx_Rx (3.3V)	2.8041mA

The serial communication operating Mode-0,1,2,3 are captured on Logic Analyzer, and shown in Figure 4.20(a),(b),(c),(d) respectively.

4.3.2 Temperature Test:

The temperature-cycling test was conducted from -10^oC to +60^oC, to establish the ASDR ASIC behavior at different temperatures. The functional tests were carried out during temperature-cycling and results were in coher-

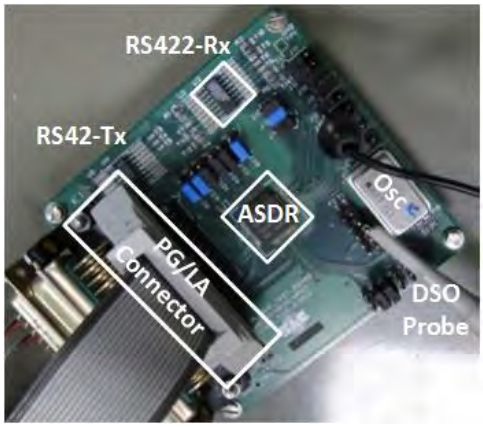


Figure 4.17: Photograph of Test Board

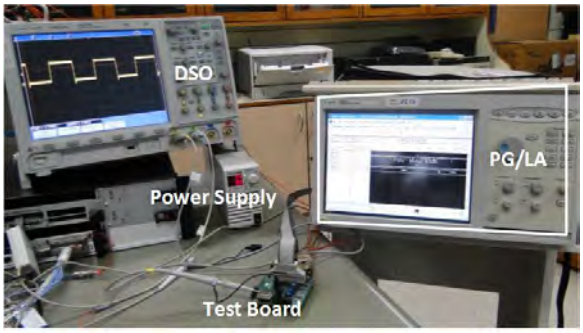


Figure 4.18: Laboratory Test Setup for testing ASDR ASIC.

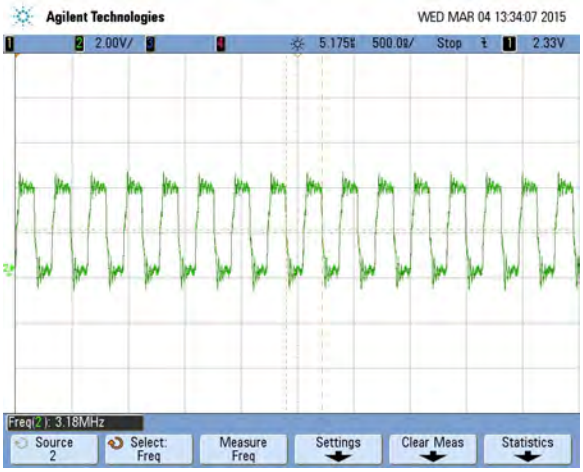
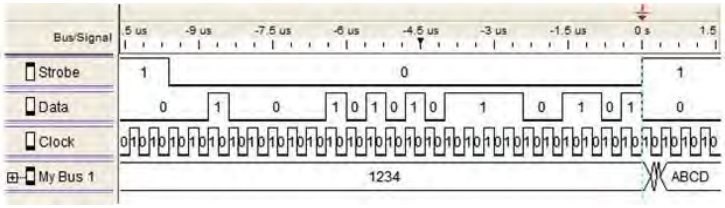
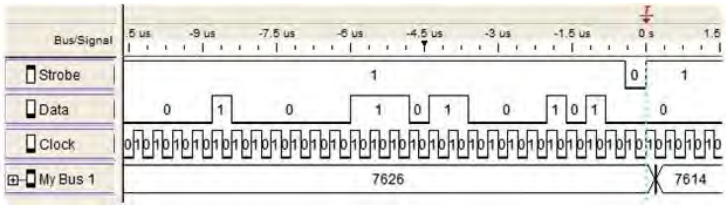


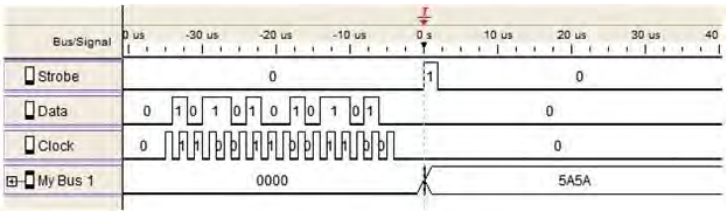
Figure 4.19: Clock-generator waveform captured on DSO



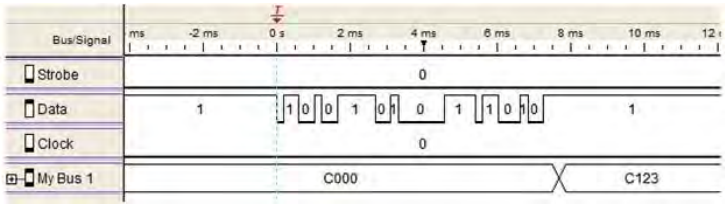
(a) Mode-0



(b) Mode-1



(c) Mode-2



(d) Mode-3

Figure 4.20: Waveform captured on Logic analyzer for (a) mode-0 [data, clock, strobe and parallel out is shown in figure]; (b)mode-1; (c) mode-2; (d) mode-3, [UART asynchronous data and parallel output is shown].

ence with simulation results. Temperature-cycling test results of the clock-generator and LVR are shown in Table-4.6. The clock-generator waveform shown in Figure 4.19 shows frequency as 3.18 MHz which is observed above $+50^oC$. The clock-generator has been designed for 4MHz, because of process variations (in transistor, resistor, capacitor), frequency is decreased by 20% to 3.18 MHz. Generally, trimming provision is kept with clock-generator

Table 4.6: Temperature Cycling test

Test Temperature	***Oscillator clock frequency***	***LVR Output***
-10^oC	3.16 MHz	1.96 V
-5^oC	3.16 MHz	1.968 V
0^oC	3.17 MHz	1.93 V
25^oC	3.17 MHz	1.927 V
50^oC	3.18 MHz	1.92 V
55^oC	3.18 MHz	1.928 V
60^oC	3.18 MHz	1.932 V

Table 4.7: Serial data handling system based on proposed ASDR ASIC

Specifications	***ASDR ASIC based system***
Chip Count	Single ASDR chip only
Area on PCB	10mm x 10mm
Power	130mW

design to nullify the process variation and bring the frequency to the desired level. Because of IOs and chip-size limitations, the trimming was not implemented in ASDR ASIC. It is evident from the test results, that the frequency of clock-generator increases as the temperature increases, which also shows that reduction in threshold-voltage of MOSFET is more prominent than reduction of mean-free-path of carrier *i.e.* mobility [71].

4.4 Conclusions

The usefulness of the design that combines functionality of RS422 receiver with synchronous/asynchronous serial protocol, is reported in this chapter. The ASDR ASIC is implemented using 0.18μm CMOS technology. The die size is around 3.5x3.5 mm^2 and it consumes 36mW quiescent power. At 10 MHz, the power is 130mW. It has 3.3V IO's while digital core operates at 1.8V. It is packaged in 64-pin CQFP and has been tested for temperature variations.The chip is designed using radiation hardening techniques of guard-ring, differential-charge-cancellation, node-splitting to get better radiation tolerance. The chip is tested at radiation dose of 500k rad and LET of

50 MeV-cm^2/mg.

We have compared the proposed ASDR ASIC system with similar systems based on standard RS422 interface devices and MCU [34] or FPGA [33]. In the papers, authors discussed the implementation details where the power and area is not reported. However MCU used in [34] is rated 600mW [72], and the FPGA in [33] is rated 2W [73] and standard RS422 chip is rated at 138mW [74]. As can be seen in the Table 4.7, the proposed ASDR ASIC can have an order of improvement in power and area. This is the first reported effort to provide integrated solution for space related applications and related parameter's in power, area quantified.

Here native MOSFETs are used to increase input-common-mode-range (ICMR) of differential-receiver. Although the use of native transistors have been reported by many authors for low-voltage applications but to the best of authors knowledge it is our novel effort of increasing ICMR with the combination of standard and native MOSFET.

It is considered that the ASIC can be useful for Microwave Payloads where multi-bit data interface from digital subsystem to RF subsystems is very essential. It has a unique combination of differential receiver, multi-mode serial-to-parallel converter, UART and addressable feature that makes it useful for control and space related applications.

Chapter 5

Radiation Test Results

Radioactive phenomenon is very high in the space. The functionality of most of the commercial integrated circuits, is destroyed because of radioactive environment present in space. Electronic components are threatened, by the presence of particles (radiations) of different energy and nature, in the space.

TID is a charge accumulation effect over a period of time, affecting the threshold voltage of MOSFET to an extent that these are either always in 'on' condition or in 'off' condition [7] [8].

Single Event Effect (SEE) is an instantaneous phenomenon in which there can be Single Event Latchup (SEL) or Single Event Upset (SEU). Once SEU is identified it can be corrected by applying reset and is often temporary in nature [6]. SEL creates a short circuit between power and ground and this may lead to over-heating or complete burnout of the device if over current protection is not available and can be catastrophic sometimes. When ions strike on an integrated circuit, charge is deposited as the particle travels through the substrate. The particle's stopping power is measured in linear energy transfer (LET) which is energy loss per unit path length (MeV-cm^2/mg).

ASDR is designed using 0.18μm process having STI and triple well technology. As shown in Table 3.1, these technology help in mitigating TID and SEE.

5.1 Radiation mitigation techniques used

Apart from these process technologies, RHBD techniques have been implemented to mitigate radiation effects are guard ring, differential charge cancellation and node splitting.

5.1.1 Guard Ring

As described in Section-3.4.2, in this layout method parallel contacts are placed between source-substrate (for NMOS), and between drain- nwell (for PMOS). So that parasitic resistor is drastically reduced and the voltage developed across these resistors will not be enough to trigger the thyristor. Guard ring structure helps in removing the ionized charge from drain/source area to VDD/VSS through low resistance path. In this design each transistor layout is done with guard ring. NMOS having guard ring connected with substrate is shown in Figure 5.1. PMOS having guard ring connected with n-well is shown in Figure 5.2. The complete differential receiver circuit

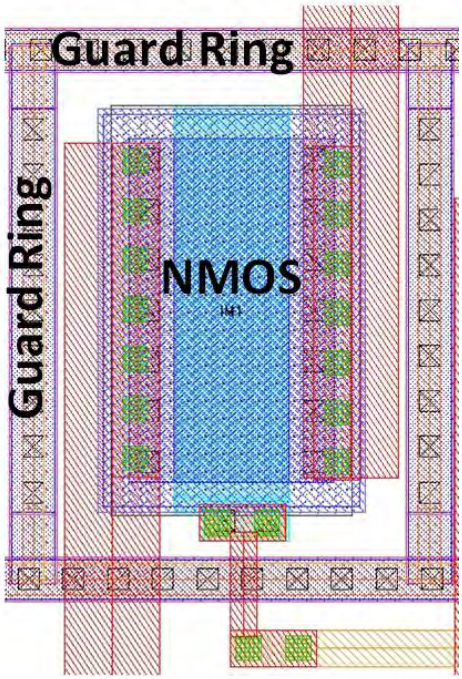


Figure 5.1: NMOS with guard ring

showing all the guard ring structure is shown in Figure 5.3.

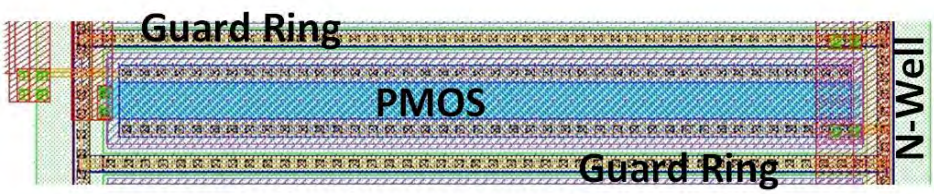


Figure 5.2: PMOS with guard ring

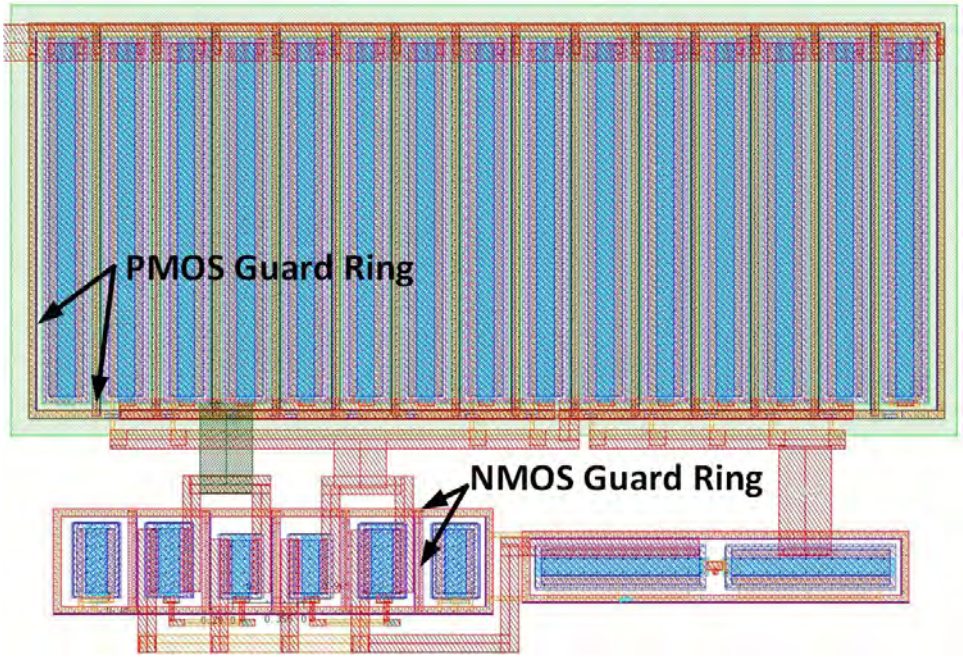


Figure 5.3: Differential receiver circuit showing guard rings

5.1.2 Differential Charge Cancellation

The charge, which is responsible for single event transient in differential circuits, is shared and converted in to common mode signal, which in turn rejected by constant tail current of differential circuit as described in Section-3.4.2. The single ended error signal is converted in to common mode signal by a simple change in layout. Generally, source terminals of differential pair

transistors are kept nearby, while in this technique drain terminals of differential pair is kept close, so that any transient on drain nodes become common to both the transistors. Keeping source terminals of differential pair close in layout is not useful as they are anyhow connected and any transient at source node is already a common mode signal. This layout technique does not have any area or matching penalty compared to common-centroid layout. Radiation sensitive area is drastically reduced if this layout technique is used and it is more effective in lower technology nodes.

This layout technique is used in all the differential circuits of this design.

5.1.3 Node Splitting

Continuous-time analog/ mixed signal circuits and switched-capacitor circuits can be hardened against single-event-effects, by creating parallel signal paths known as 'node splitting' as described in Section-3.4.2. The idea of splitting node and creating parallel signal paths has shown improvement in single-event hardness in continuous-time analog and mixed signal circuits. It is a radiation hardening by design technique at circuit/architecture level. The circuit is split/peeled in such a way that internal nodes are parallel subcircuits paths which are shorted at output and input node as shown in Figure 3.13 [59].

It is a circuit level design technique. As shown in Figure 4.3, sensitive input nodes are peeled and parallel paths are created with M2 and M4 transistors. If one path is having transient because of radiation, the other parallel path tries to keep the overall transient to average level.

5.2 Radiation Test Results

TID and SEE radiation testing was done on ASDR chip and results are described below.

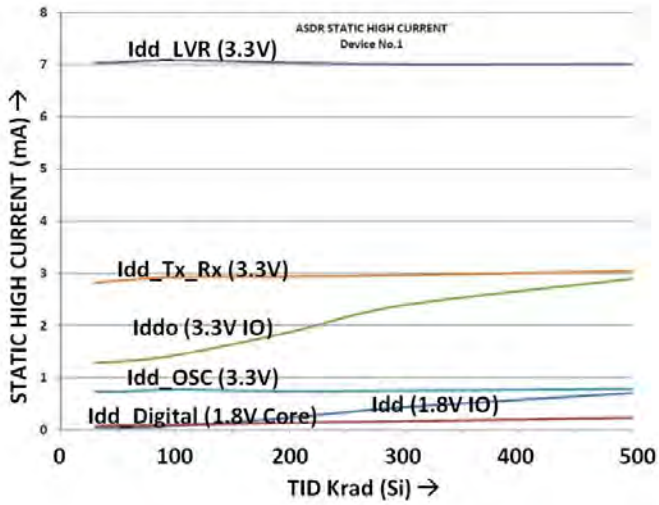


Figure 5.4: TID Test Results of ASDR having RHBD

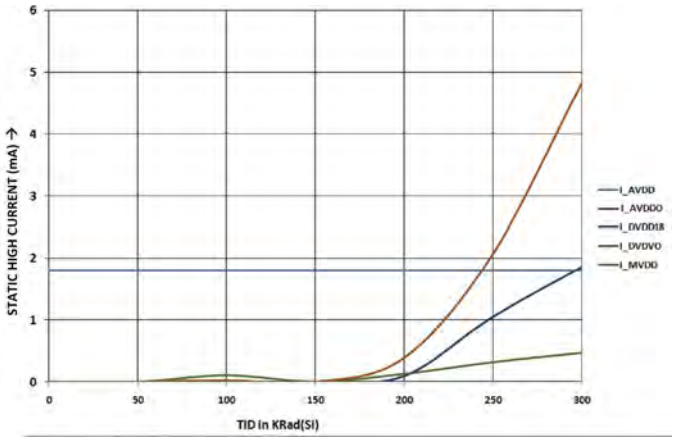


Figure 5.5: TID Test Results without RHBD

5.2.1 TID Radiation Test:

TID test on ASDR was conducted in a Gamma chamber with Cobalt (Co^{60}) source. Test was carried out up to 500K rad (dose rate = 62 rad/sec).

Test Setup

During TID test, the device was kept in power ON condition. All the input pins except TX_in and Reset_n_ext were connected to ground via 4.7kΩ resistor. The TX_in and Reset_n_ext pins were connected to 3.3V supply via 4.7kΩ resistor to keep the circuit is safe and non-reset condition. All output

pins were terminated to ground via 1M Ω resistor. Before and after the each radiation dose exposure, the device was tested for static and functional test.

Test Results

We observe that functionality of the ASIC under these conditions were OK and are shown in Figure 5.4. It shows all the supplies along with the radiation dose rate. Results indicate that I_{ddo} (3.3V IO) and I_{dd} (1.8V IO) increase slightly after 200K rad dose while all other currents were almost stable. This is a preliminary result of the test and show that current does not increase significantly. After irradiation, the devices are taken for functional tests and it passed all functionality tests. At 500K rad the current did not increase significantly but common mode input range of differential receiver was reduced. As mostly holes are trapped in gate oxide, which will reduce (increase) threshold voltage of NMOS (PMOS). The increased threshold voltage of PMOS load transistor will reduce the higher common mode voltage (CM_{High}).

Similar type of circuits were tested which were not having any RHBD techniques, and results are shown in Figure 5.5. The results show that leakage current increases from 200-400 times at 300 KRad. It describes the effectiveness of the RHBD techniques used in ASDR chip.

5.2.2 SEU/SEL Radiation Test:

To determine the Single Event Effect (SEE) sensitivity of ASDR ASIC, the test was performed in beam line at General Purpose Scattering Chamber.

Test Setup

Test setup comprises of the device under test with 3-channel power supply and a computer loaded with ASDR Test vectors. The DUT Board is designed to test the ASDR ASIC for all of its modes during SEE radiation. In this test, ASDR received differential serial signals and converted them to parallel output. During the SEE radiation test, ASDR ASIC was tested for all the operating modes (with serial data 0x0000, 0xFFFF, 0x5555, 0xAAAA, 0x1234 and 0x5678 values) and with all 5-bit address selection (0x0A and 0x15) to see the effects on different bit configuration. During this time supply currents

were also observed continuously.

Test Results

Heavy ions of Silver (^{107}Ag) and Nickel (^{58}Ni) which are Ag^{+11} and Ni^{+9} respectively, were used for the SEE testing of ASDR, as they have higher energy. During twenty minutes of test time, it was observed that Silver ions (Ag^{+11}) of 140 Mev energy, could transfer LET of 50 MeV.cm^2/mg with penetration of 17 μm. While Ni^{+9} ions of 120 Mev energy, could could transfer LET of 30 MeV.cm^2/mg with penetration of 20 μm. During the test period, current was stable and no bit flip was observed.

The SEE test results are shown in Table-5.1. Similar type of circuits were tested for SEE which were not having any RHBD techniques, and results are shown in Table-5.2. The results show that there were lot of upsets observed during the test time.

Table 5.1: SEE/SEL Test Results of ASDR

Ion Source	***Energy*** (MeV)	***LET*** $(MeV.cm^2/mg)$	***Penetration Depth***(μm)	***Fluence*** $(ions/cm^2)$	***Upset Count***
$Ni^{+9}(58)$	120	30.51	20.25	10^6	NIL
$Ag^{+11}(107)$	140	50.04	17.79	10^6	NIL

Table 5.2: SEE/SEL Test Results of non-RHBD device

Ion Source	***Energy*** (MeV)	***LET*** $(MeV.cm^2/mg)$	***Penetration Depth***(μm)	***Fluence*** $(ions/cm^2)$	***Upset Count***
$Ni^{+9}(58)$	120	30.51	20.25	10^6	88
$Ag^{+11}(107)$	140	50.04	17.79	10^6	132

5.3 Summary

Radiation hardening by design techniques (guard ring, differential charge cancellation, node splitting) have been used in the ASDR ASIC. To investigate the effectiveness of these techniques, radiation tests were conducted. ASDR could withstand total dose up to 300 Krad without any functionality loss. There was no SEE/SEL observed for LET of 50 MeV.cm^2/mg. As

ASDR design does not contain any BJT, it will not have any ELDRS effect and hence ELDRS tests were not conducted.

Chapter 6

Ultra Low Power Capacitive Power Management Unit in $0.18\mu m$ CMOS

In this Chapter, a capacitive power management unit for a DC energy harvester such as a photo-voltaic (PV) is proposed. It is assumed that the input will have a minimal voltage requirement of approximately $460mV$ and can go up to $800mV$, typical output from a PV cell. This is our initial attempt to design a novel PMU based on standard $0.18\mu m$ CMOS models to be used for applications (WSN, payload sensors) that require energy autonomy. The specifications of PMU are shown in Table 6.4.

6.1 Operating Principle

The proposed PMU circuit is shown in Figure 6.1. It has two stages of voltage doublers, each one approximately doubling the input voltage. Output of the 1^{st} stage voltage doubler will charge the capacitor C_{out1} approximately to twice the input voltage V_{in} while the output of 2^{nd} stage voltage doubler will charge the capacitor C_{out2} to V_{out} *i.e.* approximately twice the V_{DD1}. The 2^{nd} stage voltage doubler is connected to a voltage monitor that monitors the voltage across C_{out2} and regulates. If the voltage goes beyond the regulation

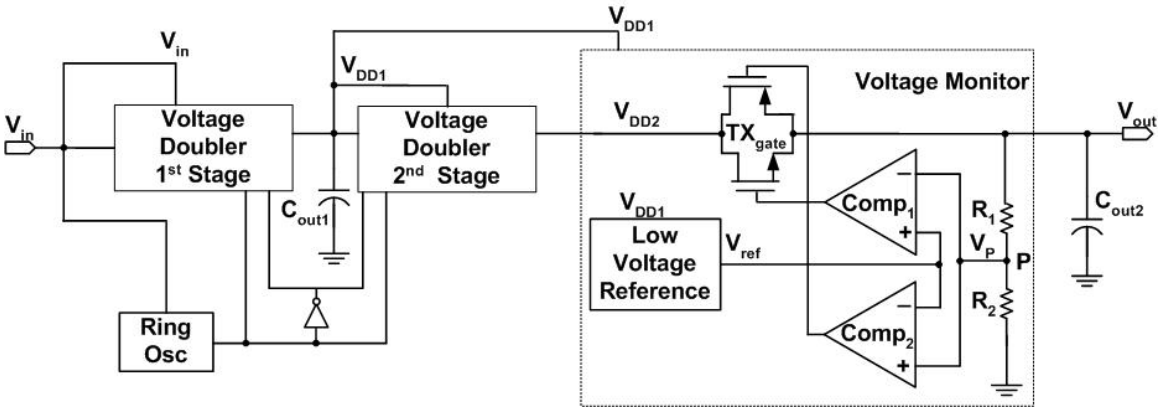


Figure 6.1: Proposed PMU Circuit

limit, the monitor disconnects the path from input V_{DD2} to C_{out2}. This voltage monitor is based on a low-voltage V_{ref} and two comparators that compares V_{ref} with the voltage at output capacitance C_{out2}. If the voltage (V_p) at node P is more than the reference voltage, the voltage-monitor will open the transmission gate, otherwise it lets the input voltage (V_{DD2}) charge the output capacitance C_{out2} to the desired voltage.

6.2 Voltage Doubler

The voltage doubler principle is depicted in Figure 6.2 [75]. Output voltage is approximately charged to twice the input voltage V_{in} (in this case the

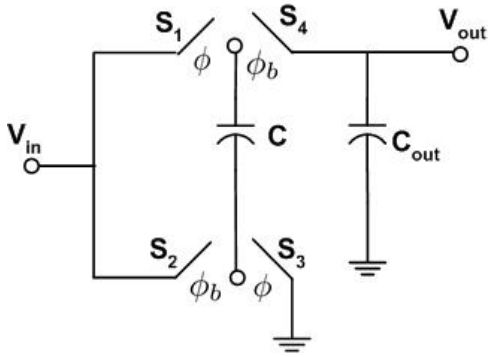


Figure 6.2: Voltage Doubler— Principle of Operation

supply), as shown in the Figure 6.2. The voltage doubling requires two clock phases ϕ and ϕ_b. In Figure 6.2, the basic operation of the voltage doubler is discussed. Switches S_3 and S_1 are closed (S_2, S_4 open), during clock phase ϕ. This will charge the capacitor C to the supply voltage V_{in}. In the next clock phase ϕ_b, the switches S_1 and S_3 are opened while S_2 and S_4 are closed.

The potential of V_{in} will be the bottom plate of the capacitor while maintaining the capacitor charge ($Q = CV_{in}$) from the previous phase. Here C is the intermediate capacitance. This results in doubling the input voltage during ϕ_b, it can be seen that the charge:

$$Q = C(V_{out} - V_{in}) = CV_{in} \tag{6.1}$$

$$V_{out} = 2V_{in} \tag{6.2}$$

In order to accommodate a load, output capacitance C_{out} is placed at the output. The equation 6.1 and 6.2 can be modified to equation 6.3 and 6.4 respectively to get the output voltage [75] as :

$$Q = (C + C_{out})V_{out} - CV_{in} = CV_{in} \tag{6.3}$$

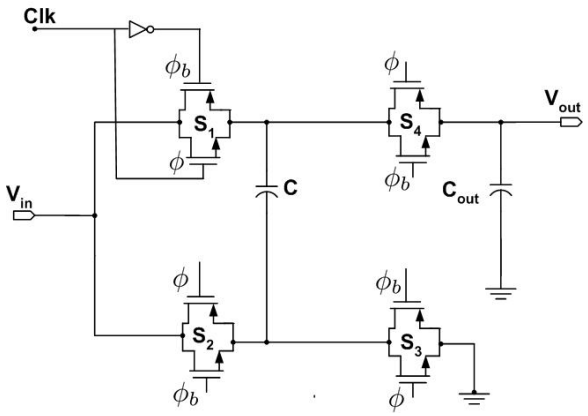


Figure 6.3: Voltage Doubler Circuit

$$V_{out} = \frac{C}{C + C_{out}}.2.V_{in} \tag{6.4}$$

In this proposed work, doubler circuit is implemented using one stage Dickson charge pump circuit, as shown in Figure 6.3. The voltage doubler has inverter and transmission-gate switches (marked $S_1 - S_4$). The inverters are for phase reversal of the clock to generate ϕ_b from ϕ and the transmission gate switches are referenced $S_1 - S_4$, exactly as in Figure 6.2. The doubler can be implemented using cross (bootstrapped) charge pump as well which shows better V_{out} vs I_{out} characteristics [76].

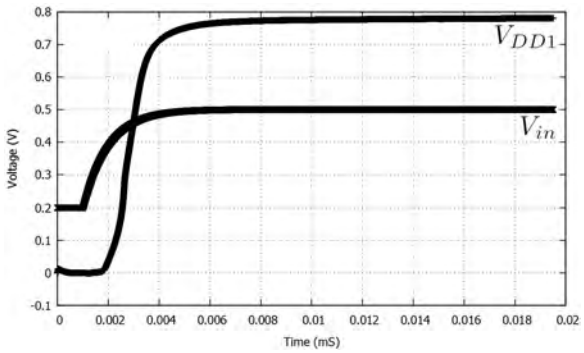


Figure 6.4: Simulation of Voltage Doubler (V_{in} varying from $200mV - 500mV$, V_{out} up-to $780mV$)

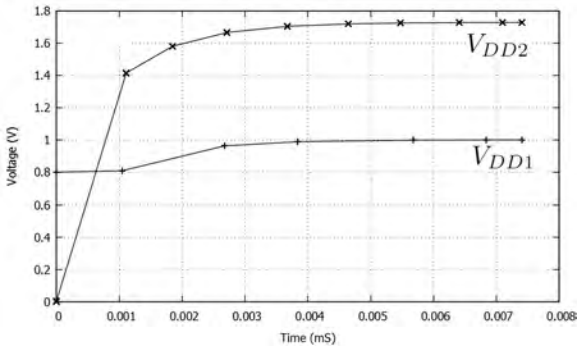


Figure 6.5: Simulation of Voltage Doubler (V_{in} varying from $780mV$ to $1V$, V_{out} Varying from $1.5V$ to $1.75V$)

The simulation result of voltage doubler circuit with an input voltage range of $200mV - 500mV$ is shown in Figure 6.4. It is seen that, the doubler

circuit starts working approximately at an input voltage of $460mV$. We can observe the gain beyond this voltage where output reaching to $780mV$ at an input voltage at $500mV$. With a second set of input voltage changing from $780mV$ to approximately $1V$ we observe that output of the second stage voltage doubler charges the C_{out} from $1.5V$ to $1.8V$ and is shown in Figure 6.5.

6.3 Ring Oscillator

For the voltage doubler to operate, a clock circuit is necessary that provides both the phases. Single stage voltage doubler discussed in this paper required frequency of $900kHz$[75]. As can be seen in Figure 6.6, this is achieved with a 5-stage RC-ring oscillator circuit. Here number of stages are kept minimum (at five) and RC delay is used to achieve the frequency of $900kHz$. Size of PMOS (24/0.18) and NMOS (12/0.8) is same for all the five stages of inverter. The oscillator works with $R = 560K\Omega$ and $C = 0.2pF$ and generates a clock frequency of $900kHz$ at $500mV$. At this voltage, the current requirement is very low, consuming $12nA$ and hence is adopted for the PMU. The simulation results of ring oscillator are shown in Figure 6.7. Both stages of the voltage doubler circuit is being fed from the same ring oscillator.

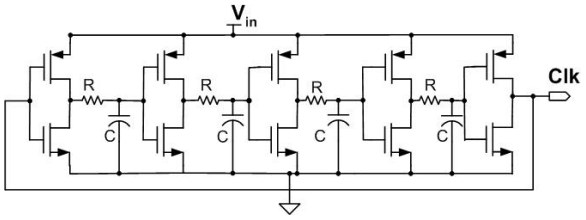


Figure 6.6: Ring Oscillator Circuit

6.4 Voltage Monitor

The voltage monitor consist of a low voltage reference (V_{ref}), two comparators, transmission gate (TX_{gate}) and a resistor network as shown in Figure

6.1. The voltage monitor provides a voltage within two specific levels at the output. In the proposed design, the higher level and the lower level is fixed at $2.0V$ and $1.5V$ respectively. This voltage level is maintained by the two comparators ($Comp_1$ and $Comp_2$ and the TX_{gate}. Both the comparators use a stable V_{ref} and compares a part of output voltage V_p through the ratioed logic using R_1 and R_2. The output of the comparators drive the TX_{gate} that ensures the V_{out} to be within $1.5V$ to $2.0V$. For example, if the $V_p < V_{ref}$, output of $Comp_1$ will be high (NMOS will turn ON), and output of $Comp_2$ will be low (PMOS will turn ON). This will provide a direct path from the input (V_{DD2}) to output (V_{out}). In case of $V_p > V_{ref}$, both the NMOS and PMOS are off, thereby no charging at C_{out2}. As V_p changes, repetition of the above cycle occur. The individual circuits of low voltage reference, Op-Amp and comparator are discussed in the following sub-sections.

6.4.1 Low Voltage Reference (V_{ref})

The reference circuit consists of an op-amp, BJTs Q_1 to Q_3, and MOSFETs M_a to M_e as shown in Figure 6.8. The reference circuit works on principle of CTAT (Complimentary To Absolute Temperature) and PTAT (Proportional To Absolute Temperature), where V_{BE} of Q_1 is inversely proportional to the temperature that exhibits CTAT where

$$V_{BE@Q_1} = V_T ln(\frac{I_{C@Q_1}}{I_S}) \tag{6.5}$$

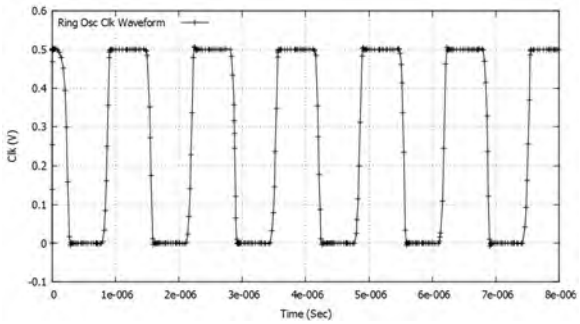


Figure 6.7: Simulation Results of the Oscillator @ $900kHz$

while PTAT is exhibited by $\triangle V_{BE}$.

$$\triangle V_{BE} = (V_{BE@Q2} - V_{BE@Q1}) \tag{6.6}$$

$$\triangle V_{BE} = V_T ln(\frac{I_{C@Q_2}}{I_S} . \frac{I_S}{I_{C@Q_1}}) = V_T ln(m) \tag{6.7}$$

Where ($I_{c@Q_2} = m \times I_{c@Q_1}$) (area of Q_2 is m times the area of Q_1), V_{BE} is base to emitter voltage , I_C is collector current, I_S is saturation current of a BJT and V_T is thermal voltage. These two temperature-coefficients cancel each other to give nominally zero temperature-coefficient. Transistor ratios are shown in Table 6.1.

Table 6.1: Transistor ratios for Low Voltage Reference Circuit

Transistors	**Type**	**W/L in μm/μm**
M_a	NMOS	40/1
M_b	NMOS	40/1
M_c	PMOS	20x64/1
M_d	PMOS	20x64/1
M_e	PMOS	20x64/1

The V_{ref} circuit consumes current of approximately $7\mu A$. The simulation results of the low voltage V_{ref} is shown in Figure 6.9. As can be seen in

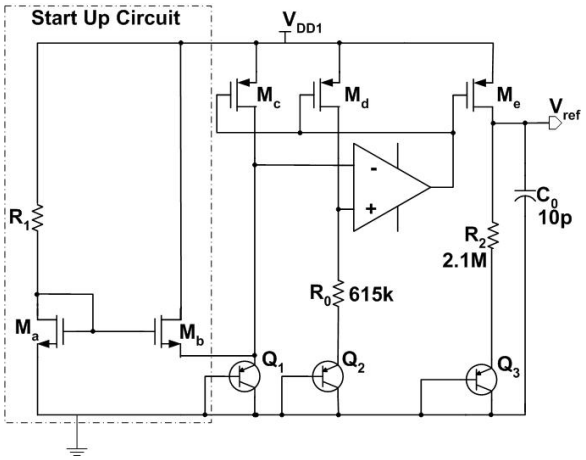


Figure 6.8: Low Voltage Reference Circuit

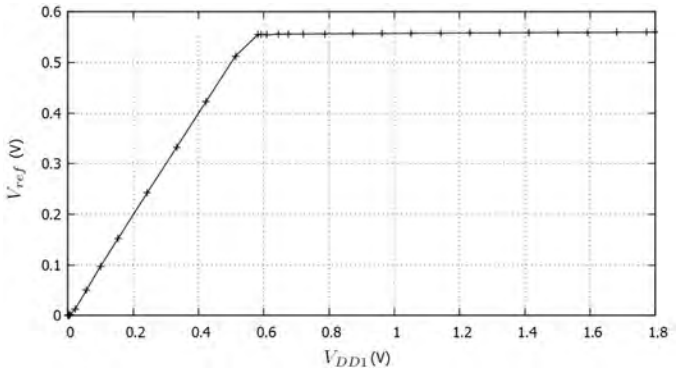


Figure 6.9: Simulation Results for Low Voltage Reference V_{ref}

Figure 6.9, the crossover of V_{in} and V_{ref} is at $600mV$. The effect of PTAT and CTAT can be observed from a stable V_{ref}. Here sub-bandgap voltage reference (V_{ref}) is driven from $V_{DD1}(\approx 0.8-1.2V)$ while it also can be driven from $V_{DD2}(\approx 1.4-1.8V)$ as described in [77], [78] and [79].

6.4.2 Op-Amp

The reference circuit uses a low voltage operational amplifier circuit as shown in Figure 6.10. It is a two stage op-amp with pole splitting compensation. Input stage is PMOS differential pair and output stage is a common source amplifier. Transistor ratios are given in Table 6.2. The op-amp provides gain of $23dB$ at $500mV$ supply. The gain and phase plot are shown in Figure 6.11, which shows UGB at $150kHz$ and Phase-Margin of 70^o.

6.4.3 Comparator

The circuit of comparator is shown in Figure 6.12. The circuit is derived from the low voltage op-amp discussed in [80]. In the voltage monitor circuit, the comparator acts when the output voltage on capacitor goes beyond $2V$, then it will generate switching signals for transmission gate. This will in effect disconnect the path from input to output and ensure the voltage to ripple within a range- say $1.5V$ to $2V$ in our proposed PMU. The comparator circuit takes current of around $6\mu A$.

Table 6.2: Transistor ratios for Op-Amp circuit

Transistors	**Type**	**W/L in μm/μm**
M_1	NMOS	35.66/1.5
M_2	NMOS	35.66/1.5
M_3	PMOS	2x64.87/2
M_4	PMOS	2x64.87/2
M_5	PMOS	6x81.95/2.5
M_6	PMOS	30x81.95/2
M_7	NMOS	10x35.66/2
M_8	PMOS	3x81.95/2.5
M_9	NMOS	20.95/2.5
M_{10}	NMOS	20.95/2.5

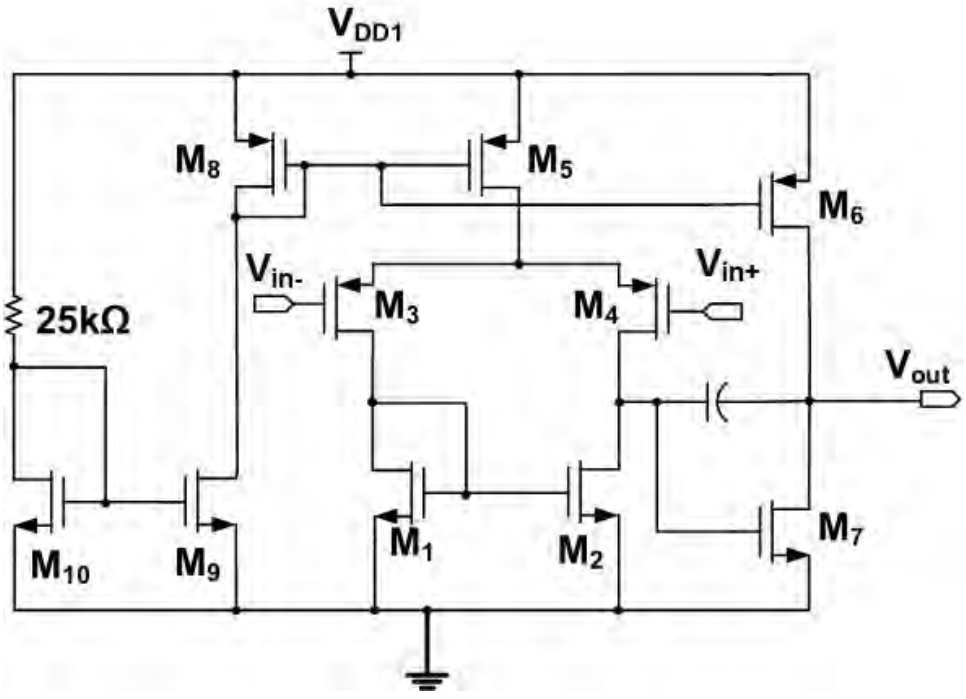


Figure 6.10: Op-Amp Circuit

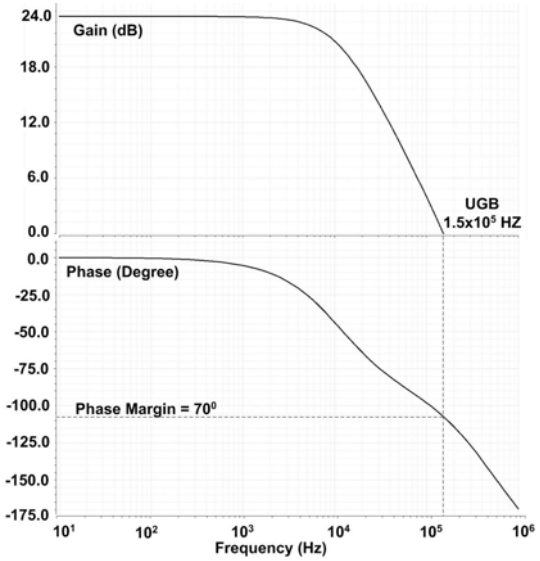


Figure 6.11: Gain and Phase plot of Op-Amp

6.5 Radiation mitigation techniques used in PMU

RHBD techniques have been implemented to mitigate radiation effects in PMU. All the PMOS and NMOS are enclosed in guard ring. All the differ-

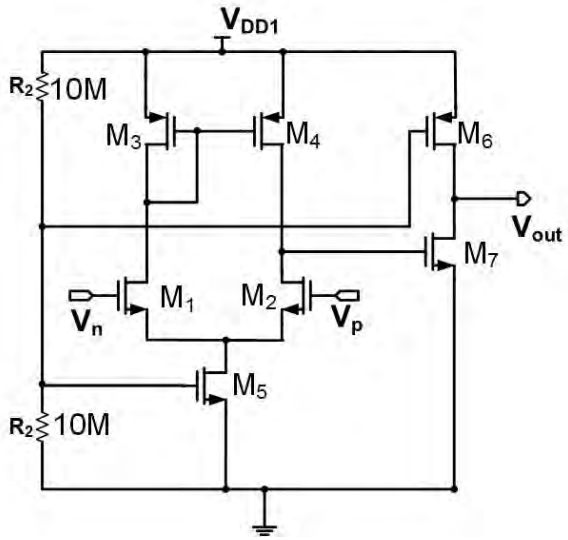


Figure 6.12: Comparator Circuit

Table 6.3: Transistor ratios for Comparator circuit

Transistors	**Type**	**W/L in μm/μm**
M_1	NMOS	8x5/1
M_2	NMOS	8x5/1
M_3	PMOS	8x12.5/0.4
M_4	PMOS	8x12.5/0.4
M_5	PMOS	10x5/1
M_6	PMOS	40x8.235/10
M_7	NMOS	6/1

ential circuits layout is done with differential charge cancellation technique. The complete layout is shown in Figure 6.13. Generally clamping diode (MOSFETS as diode connected) circuits are implemented for electro-static-discharge (ESD) protection. As can be seen in the layout, simple pads are used without ESD circuit. So extra care will be taken while handling these devices. The testing will be carried out on properly grounded anti-static mats using anti-static wrist strap, the devices will be stored in anti-static bags only.

6.6 Results and Discussion

Table 6.4: PMU Specifications

Parameter	***Specification***
Input voltage range	400-800mV
Output Voltage	1.8V
Load Current	1mA
Peak Power Efficiency	64% @ 500μA

Figure 6.14, shows the simulation results of PMU. The input voltage, Vin varies from 0-800mV (typically an output of a solar cell at indoor lighting conditions at 200 lux gives an output of 400mV) for the first voltage doubler. The output of first voltage double, Vdd1 varies from 1-1.25V and is input to second stage. The output voltage, Vout is around 1.8V as most of the standard CMOS circuit operates at 1.8V. Voltage reference circuit provide the

Table 6.5: Current and Voltage of different Sub-blocks

Individual Blocks	Voltage(V)	Current(A)
Voltage Reference	$800mV - 1.5V$	$7\mu A - 20\mu A$
Op-Amp	$800mV$	$1\mu A$
Comparator	$800mV - 1.5V$	$6\mu A - 20\mu A$
Ring Oscillator	$500mV$	$12nA$
Voltage Doubler 1	$500mV$	$1\mu A$
Voltage Doubler 2	$800mV$	$2\mu A$
PMU	$@500mV$	$22\mu A$

reference voltage of 600mV. It has power efficiency of around 64%. The load regulation and line regulation are shown in Figure 6.15 and 6.16 respectively.

The specifications and current consumption at different voltages of the

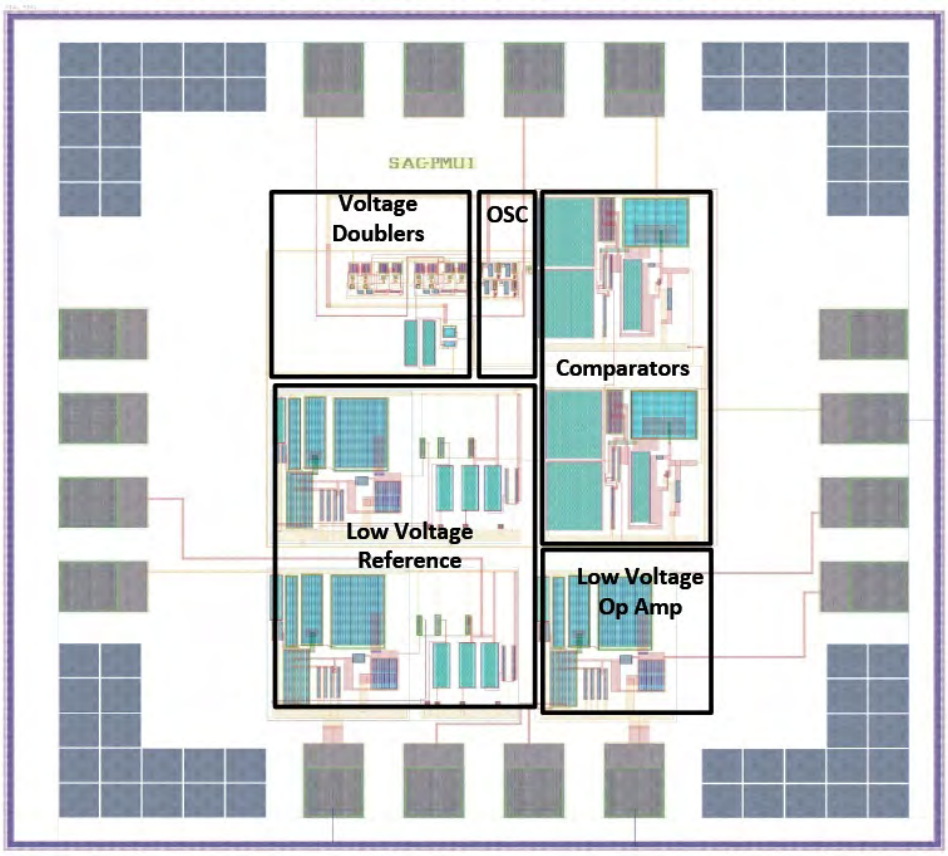


Figure 6.13: Layout of PMU

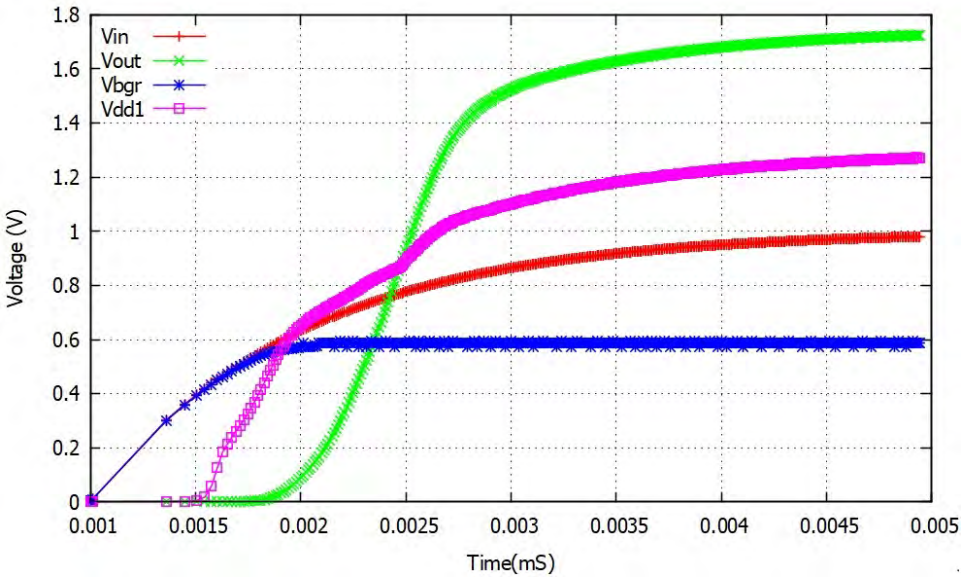


Figure 6.14: Output of the PMU

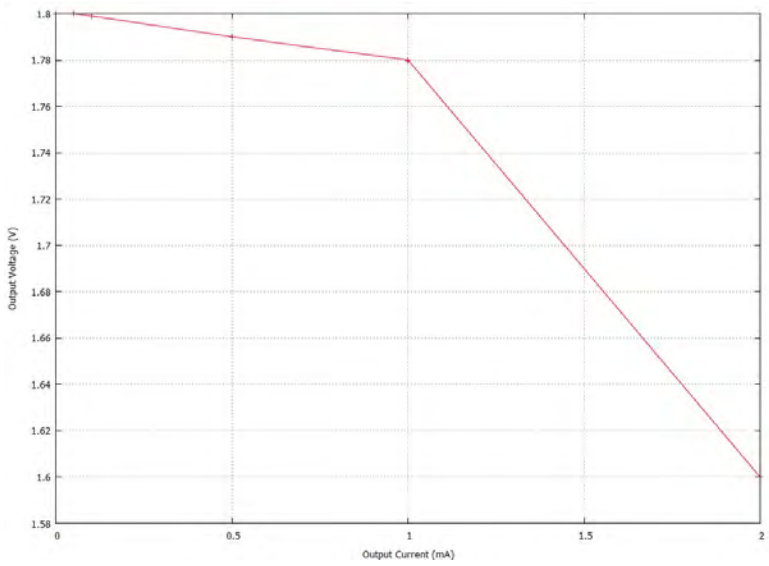


Figure 6.15: Load regulation

individual blocks of the PMU is provided in Table 6.4 and 6.5 respectively.

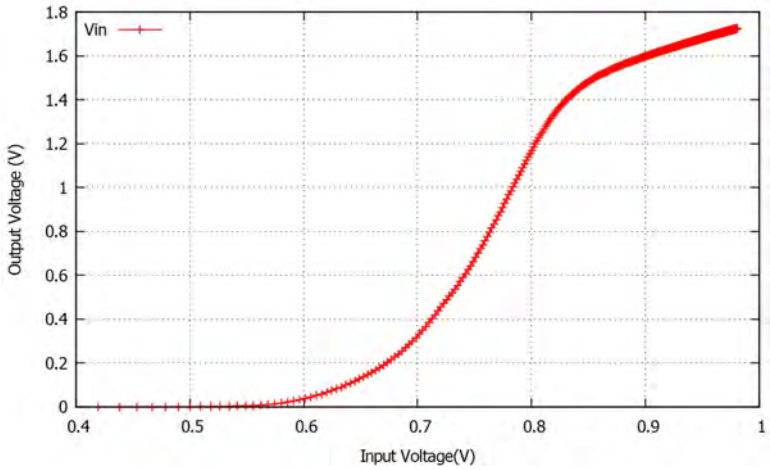


Figure 6.16: Line regulation

6.7 Summary

A new ultra low power, Power Management Unit is proposed which works on 460-800mV input voltage and gives 1.8 volt. It has different modules od voltage double, ring oscillator, low voltage reference and comparator. The voltage reference and the comparator consume the most current and is the subject of our future work to optimize it to nano-ampere consumption. The total power consumption of our proposed PMU is $22\mu A$ at $500mV$ ($11\mu W$).

Chapter 7

Conclusion and Future Work

This report details out the objective of designing circuit components, for wired and wireless methods of temperature sensing shown in Figure 1.1.

For wired approach, addressable synchronous asynchronous differential receiver (ASDR) circuit is designed. ASDR implements the RS422 electrical standard for differential-serial-data reception and has multi-mode synchronous-asynchronous serial data handling capability. The 16-bit parallel data can be generated from this serial data. Combination of these functionalities is not available commercially in a single chip and hence a single chip solution is designed. ASDR ASIC is implemented using $0.18\mu m$ CMOS technology. The die size is around 3.5x3.5 mm^2 and it consumes 36mW quiescent power. At 10 MHz the power consumption is 130mW. It has 3.3V IOs while digital core operates at 1.8V. It has been packaged in 64-pin CQFP and tested. Radiation hardening techniques of guard-rings, node-splitting and differential-charge-cancellation have been used in this design to get better radiation performance. Here we have used native transistors for increasing voltage headroom. The chip is tested at radiation dose of 500k rad and LET of 50 MeV-cm^2/mg. It is considered that the ASIC will be very useful for Microwave Payloads where multi-bit data interface from digital subsystem to RF subsystems is very essential and it requires large harnesses. It has a unique combination of differential receiver, multimode serial-to-parallel converter, UART and addressable feature that makes it a useful design for space

and related applications.

For future scope the ASDR can be tested for higher LET values and if required some more radiation mitigation techniques like 'enclosed layout transistor' and DICE structure can be implemented to make it more radiation hardened.

For wireless approach, power-management-unit (PMU) is designed that can work with DC energy harvesters like photovoltaic and thermo-electric generators. The PMU can work from very low voltages of $460mV$ and can output a stable voltage output for the circuits to operate reliably. The proposed capacitive PMU circuit has an added advantage of operating from cold start without the need of any additional circuit for jump-start compared to similar circuits in [45] and [46] , where they need jump start voltages to start the PMU. radiation hardening technique of guard-rings and differential-charge-cancellation have been used in this design to get better radiation performance. Quantification of the harvesting efficiency of the harvesters along with the peak efficiency is important for PMUs and is left as future work. The proposed PMU consumes $11\mu W$ at an input voltage of $500mV$. The power consumed is comparable to the power cited in [45], [47] and [48].

The voltage monitor consumes the greater part of this power and is the scope of our future work. Apart from reducing power number, some more radiation mitigation techniques like 'enclosed layout transistor' and DICE structure can be implemented to make this PMU design more radiation hardened.

Future work involves the board design and complete system implementation using ASDR and PMU chips as shown in Figure 1.1. Further to that the complete system can be designed as an SOC, where temperature sensor, micro-controller and ASDR be on the same chip. In similar fashion for wireless approach, the complete system comprising temperature sensor, micro-controller, zigbee (RF) can be designed to be on the same chip.

In the Appendix of this report, our initial work on "a new low voltage differential current conveyor" is described. As low power and hence low voltage is main design consideration now a days, a low voltage circuit for

DDCC (LVDCC) has been proposed for supply voltage of ±1.5V with a good performance. It gives bandwidth of around 12MHz. Which gives output swing from -1.3 to +1.4, which is nearly rail-to-rail. Proposed low voltage circuit has been used to implement a current amplifier for gain of 10 and seen that it gives good results with bandwidth of 1.2 MHz. This idea can be extended to make a fully differential current conveyor (FDCC) also.

Appendix A

Novel Low Voltage Differential Current Conveyor

A.1 Introduction to Current Conveyor

A basic Current conveyor is a three port circuit block. It can be configured in different specific circuits and can be used in many analog signal processing application [27]. Like operational amplifier, the current conveyor also simplifies circuit design if used as circuit building block and thus complex circuits can be implemented using it. This together with the fact that the actual terminal behavior of the current conveyor is very near to ideal, just like operational-amplifier. It can provide a higher gain bandwidth product than a corresponding op-amp circuit [81]. In addition, instrumentation amplifier have been successfully developed using current conveyor. One can convert specific type of active-RC circuits into equivalent current conveyor circuits. An important feature of this approach is that it preserves the sensitivities of the original active-RC circuit [81]. The input-output characteristics of current conveyor can be depicted in matrix equation as-

$$\begin{pmatrix} i_y \\ v_x \\ i_z \end{pmatrix} = \begin{pmatrix} 0 & a & 0 \\ 1 & 0 & 0 \\ 0 & c & 0 \end{pmatrix} \begin{pmatrix} v_y \\ i_x \\ v_z \end{pmatrix}$$

This is a simple and efficient way to represent the current conveyor characteristics and used mostly in the literature. All instantaneous quantities are represented by the variables. The nature or *generation* of the conveyor is denoted by the value of a. A positive transfer conveyor will have a positive value of c. This becomes a conveyor with negative transfer when c is negative. Depending on the values of a and c, current conveyors are classified as below

1. Current Conveyor–I

   - a=1
   - c=$\pm$1
   - This is called as first generation current conveyor.

2. Current Conveyor–II

   - a=0
   - c=$\pm$1
   - This is called as second generation current conveyor.

3. Current Conveyor–III

   - a=-1
   - c=$\pm$1
   - This is called as third generation current conveyor.

where sign denotes direction of the current. All the three generations of the current conveyor are described in the following sections.

A.2 Current Conveyor–I

Initially introduced as a three port device, the first generation current conveyor (CCI) [82] symbol can be seen in Figure A.1. It can be further classified

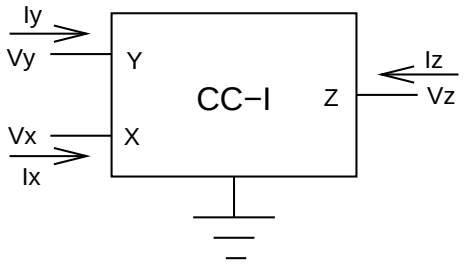


Figure A.1: Symbol of the current conveyor

as positive and negative current conveyor depending on polarity of the current. Characteristic equations are summarized below.

$$\begin{aligned} i_y &= i_x \\ v_x &= v_y \\ i_z &= \pm i_x \end{aligned}$$

1. Positive Current Conveyor–I (*CCI+*)

   - $i_z = +i_x$
   - When both i_x and i_z flow into the conveyor, it is denoted as *CCI+*

2. Negative Current Conveyor–I (*CCI-*)

   - $i_z = -i_x$
   - In current conveyor–I, if i_z flows opposite to the direction of i_x, it is denoted as *CCI-*

The operation of this device is such that if a voltage is applied to terminal Y, the same potential is mirrored at the node X. And current through the node Y (i_y), will be similar to input current being forced into node X, i_x. Similarly i_z will follow i_x. As can be seen, current being forced into port X is not dependent on the potential at X, as it is decided by voltage at Y. In the same way the current i_x will set the current i_y, which is not controlled by voltage at Y. And hence the behavior of node Y will be of a dual virtual open-circuit, and node X will be of virtual short-circuit input. *CCI* is widely used in wide band current measurement and negative impedance converter.

A first order *CMOS* implementation of *CCI+* is shown in Figure-A.2 [83]. Due to mirroring action of M2–M3, currents i_x and i_y are equal. Voltage at X and Y terminal is almost[1] same which is threshold voltage added to the drain to source saturation voltage. Currents i_z and i_x are same because of mirror M3–M4. As i_x and i_Z are in the same direction, it is a *CCI+* circuit.

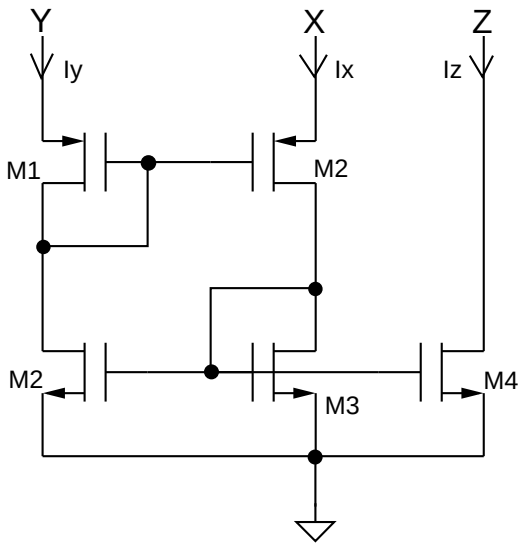


Figure A.2: CMOS implementation of positive current conveyor–I

A.3 Current Conveyor–II

A second generation of the current conveyor was introduced [27], to cater to more applications. In this version there is no current flowing in to node Y. This building block has since proven to be more useful than *CCI*.

Black box representation for *CCII+* is shown in Figure A.3. It also can be classified as positive and negative depending on polarity of current like *CCI*. Characteristic equations are summarized below.

$$\begin{aligned} i_y &= 0 \\ v_x &= v_y \\ i_z &= \pm i_x \end{aligned}$$

[1]Magnitude of the threshold voltage for PMOS and NMOS are not same.

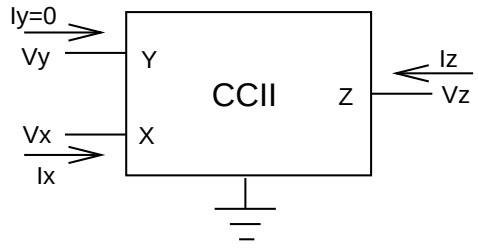


Figure A.3: Black box representation for current conveyor–II

1. Positive Current Conveyor–II (*CCII+*)

   - $i_z = +i_x$
   - When both i_x and i_z flow into the conveyor, it is denoted as *CCII+*

2. Negative Current Conveyor–II (*CCII-*)

   - $i_z = -i_x$
   - In current conveyor–II, if i_z flows opposite to the direction of i_x, it is denoted as *CCII-*

Thus an infinite input impedance is seen at node Y. The voltage at Y is mirrored at node X and hence zero input impedance is seen at node X. The current at output node Z, i_z is conveyed from node X current (i_x). The polarity of i_x will determine CCII+ or CCII-.

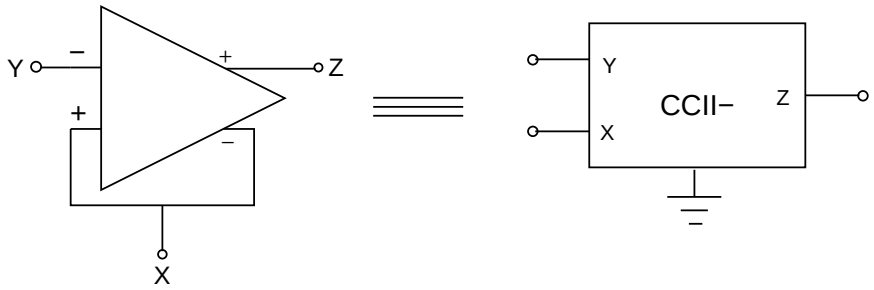


Figure A.4: Correspondence between ideal op-amp and CCII-

Earlier op-amp was used to realize *CCII* but that was not the convenient building block to realize *CCII* as op-amp is a voltage mode device while the

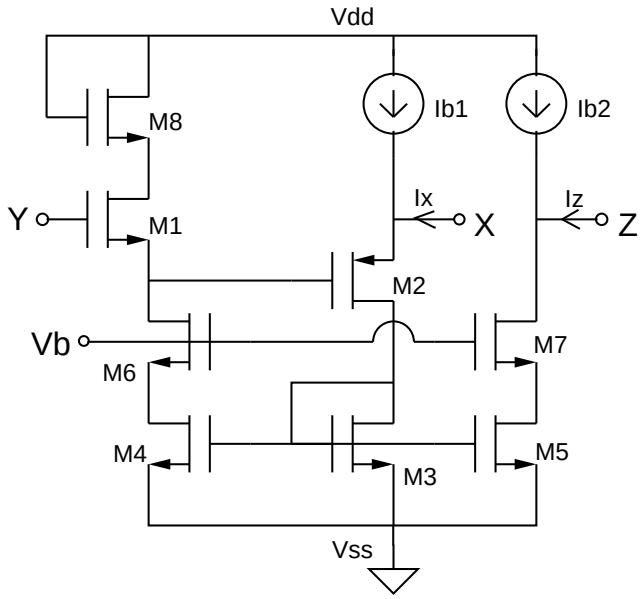


Figure A.5: Circuit implementation for positive current conveyor–II

current conveyor is a current mode device. Correspondence between an ideal op-amp and *CCII-* is shown in Figure A.4 [83].

In the past decade many CMOS implementations have been reported [84]–[88]. A circuit for *CCII+* is shown in Figure A.5 [84]. In the circuit, Y terminal is gate of the transistor M1, i_y is nearly zero. Voltage v_x and v_y are almost same and V_{TH} above the drain voltage of M6. Transistors M3–M5 forms basic current mirror and hence i_x and i_z are equal. Transistor M7 increases output impedance and M8 works as a current source.

Many analog functions can be synthesized using CCII circuits because of its voltage and current conveying properties [81]. Some application of current conveyor to active network synthesis are listed below [89].

1. Current controlled voltage source
2. Current controlled current source
3. Voltage controlled current source
4. Voltage controlled voltage source
5. Floating inductance synthesis

6. Negative impedance converter

7. Biquad filter

8. Oscillator

Some application of current conveyor to analog computation are listed below [29].

1. Current divider

2. Current squarer

3. Current summer

4. Current integrator

5. Current multiplier

6. Current differentiator

7. Current square rooter

In the last decade efforts have been made by people to make CCII more versatile for the analog and mixed mode applications. To make CCII more useful for mixed mode applications, differential processing feature has been added to it. There are two advanced version of CCII have been reported in the literature with differential processing capability [28].

1. DDCCII

    - It is known as *differential difference current conveyor–II.*

2. FDCCII

    - It is known as *fully differential current conveyor–II.*

A.4 Differential Difference Current Conveyor (DDCC)

DDCC is introduced by Chiu [27]. Author has combined the advantages of differential difference amplifier (DDA) and the second generation current conveyor(CCII), making a new circuit named DDCC. It has been shown that DDCC based circuits offer a competitive design choice to CCII- based and DDA–based circuits.

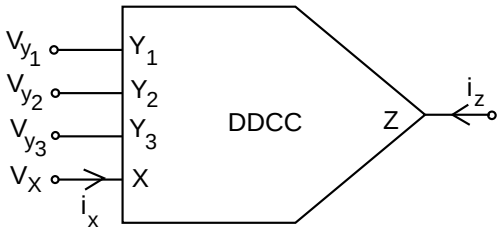


Figure A.6: Symbol of the DDCC

The symbol of DDCC is shown in Figure A.6. DDCC is a five port circuit block and the port characteristics are given as [27]

$$\begin{aligned} i_z &= \pm i_x \\ v_x &= v_{y_1} - v_{y_2} + v_{y_3} \\ i_{y_3} &= 0 \\ i_{y_2} &= 0 \\ i_{y_1} &= 0 \end{aligned} \tag{A.1}$$

Here DDCC- and DDCC+ are referred as inverting and non–inverting configuration respectively. Here if $v_{y_3} = 0$, Eq.(4.1) is same as Eq.(2.1). Here Y_3 terminal can be used for biased signal processing.

The CMOS DDCC+ circuit is shown in Figure A.7

The input differential stages are realized with M1–M2 and M3–M4. Differential current are converted to single ended by current mirror (M5–M6) which also provides high gain to differential stage.

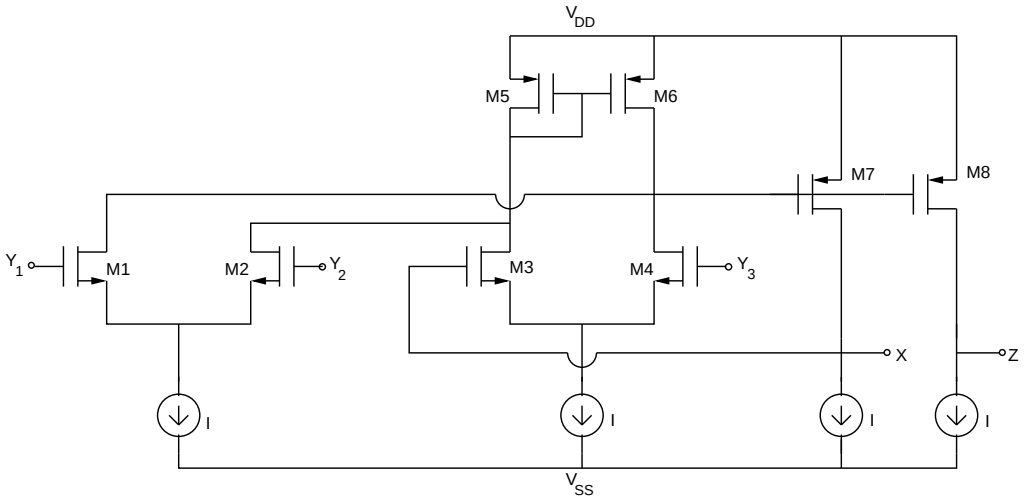


Figure A.7: CMOS, non inverting DDCC (DDCC+)

The voltage at output of this amplifier is given by

$$\mathrm{V_x} = \mathrm{A_0}[(\mathrm{V_{y_1}} - \mathrm{V_{y_2}}) - (\mathrm{V_{G_3}} - \mathrm{V_{y_3}})]$$

Where $\mathrm{V_{G_3}}$ is the gate voltage of M3 and $\mathrm{A_0}$ is the open–loop gain of the amplifier. The gate of the M3 is connected to output node (X) of the gain stage, to provide negative feedback.

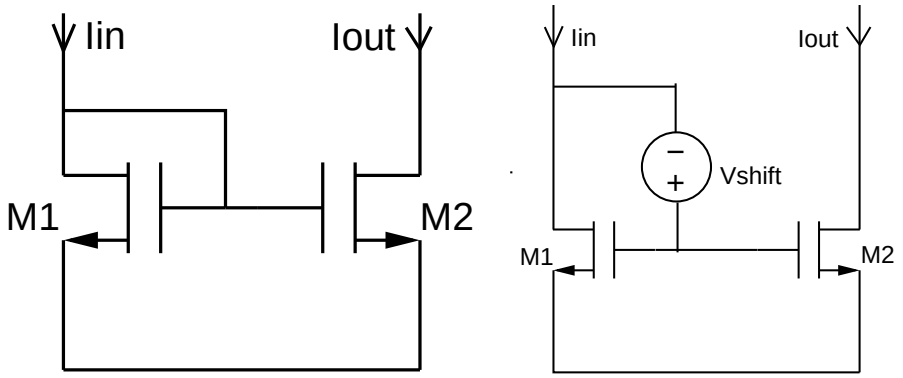
If the amplifier's open–loop gain is much larger than one, the voltage at terminal can be given by

$$\mathrm{V_x} = \frac{\mathrm{A_0}}{\mathrm{A_0} + 1}[\mathrm{V_{y_1}} - \mathrm{V_{y_2}} + \mathrm{V_{y_3}}] \approx [\mathrm{V_{y_1}} - \mathrm{V_{y_2}} + \mathrm{V_{y_3}}]$$

The current of the transistor M7 is mirrored in transistor M8, and hence output terminal Z carries current I as shown in Figure A.7. The currents i_x and i_z flow simultaneously towards or away from the DDCC and hence it is a DDCC+.

A.5 Low Voltage Current Mirror

The current-mirrors (CM)are inherent to analog/mixed signal circuits. Many structures of current mirrors are available like simple CM, Widlar CM, Wilson CM, modified Wilson CM, cascode CM, etc. These current mirrors have high output voltage swing [90] but input voltage swing is not high enough for low voltage applications. These current mirror uses diode connected configuration of the input transistor. And because of this, at least one threshold voltage is required at input (v_{in}).



(a) Basic current mirror

(b) Corresponding low voltage current mirror

Figure A.8: Current mirror

$$v_{\text{in}} \geq (V_{\text{th}} \approx 0.7V)$$

A conventional current mirror is shown in Figure A.8(a). Gate-Drain of M1 are connected. The current i_{in} is generated by input voltage v_{in} at the input port. M1 operates in saturation mode, and the current through it will decide the value of v_{in}. The input impedance will be dependent on transconductance of M1 (g_{m_1}).

Following equation describes v_{in} for this structure:

$$v_{\text{in}} = V_{\text{tn}} + \sqrt{\frac{2i_{\text{in}}}{\beta_1}}$$

The value of v_{in} can not be less than V_{tn}, threshold voltage of NMOS. Where $\beta_1 = \frac{\mu_n C_{\text{ox}} W_1}{L_1}$.

Different types of low voltage current mirrors are described in [91] and [92]. Few of them used MOSFETs driven by bulk, having disadvantage of lower input current range ($i_{\text{in}} < 150\mu A$) and lower bandwidth (BW < 100MHz) [93].

We have used a low voltage current mirror given by [94], which uses level–shifter[2] technique.

The LVCM (Low voltage current mirror) is shown in Figure A.9. It uses M1 and M2 just like conventional current mirror as in Figure A.8(a). The low bias current (I_{bias_1}) ensure sub–threshold operation of level–shifter M4.

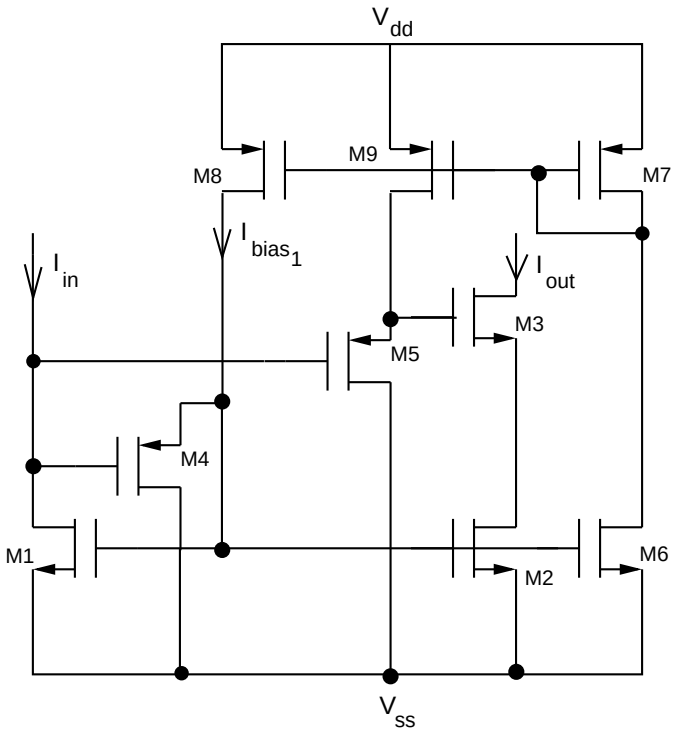


Figure A.9: LVCM Structure

A appropriate bias is given to M3 by second level–shifter M5. Output impedance (R_{out}) is because of cascode action of M3 . Input current (i_{in}) in M1 is mirrored in to M2.

[2]Shifting level with the help of equivalent voltage source

Input voltage at M1 is given by

$$v_{\text{in}} = V_{\text{tn}} + \sqrt{\frac{2i_{\text{in}}}{\beta_1}} - V_{\text{gs}_4}$$

Where $\beta_1 = \frac{\mu_n C_{\text{ox}} W_1}{L_1}$ and V_{gs_4} is gate–to–source[3] voltage of M4.

$$V_{\text{gs}_4} = \eta V_{\text{T}} + ln \frac{I_{\text{bias}_1} L_4}{I_{\text{DO}_4} W_4}$$

V_T is thermal voltage ($= \frac{kT}{q}$) and $1 < \eta < 2$.

Input impedance of the LVCM is given by

$$R_{\text{in}} \approx \frac{1}{g_{m_1}}$$

Output impedance of the LVCM

$$R_{\text{out}} \approx \frac{g_{m_4} g_{m_2}}{g_{d_4} g_{d_2}^2}$$

The minimum voltage at output will be

$$v_{\text{out}} = V_{\text{ds}_2(\text{sat})} + V_{\text{ds}_3(\text{sat})}$$

Current transfer can be given as:

$$\frac{I_o(S)}{I_{in}(S)} \approx \frac{1}{1 + \frac{sC_{in}}{g_{d_1}}}$$

Offset current (I_{offset}) is important in low voltage current mirror and sets the lower limit for I_{in}. When $I_{\text{offset}} = 0$, V_{ds_1} must be zero but due to level–

[3]In subthreshold region drain current $I_{d_n} = \frac{I_{\text{DO}} W e^{\frac{V_{\text{gs}} - V_{tn}}{\eta V_T}}}{L}$

shifting action of the M4, M2 has some voltage at its gate. If I_{in} is zero, M2 will carry a sub-threshold current. This offset current is given by

$$I_{\text{offset}} = I_{\text{bias}_1} \frac{W_2 L_4 I_{\text{DO}_2}}{L_2 W_4 I_{\text{DO}_2}} e^{\frac{\Delta V_t}{\eta V_T}}$$

Here I_{offset} can be adjusted to the requirements, through the proper selection of W and L. Mismatch $\Delta V_t (\approx V_{tn} - V_{tp})$ in threshold voltages are governed by process technology. The minimum value of the I_{offset} is

$$I_{\text{offset}} = I_{\text{bias}_1} \frac{W_2 L_4 I_{\text{DO}_2}}{L_2 W_4 I_{\text{DO}_2}}$$

Appropriate values for the W/L ratio of M4, M2 and lower value of I_{bias_1} can give lower I_{offset}. Simple form of the LVCM, shown in Figure A.10 can also be used in place of the complete circuit (Figure A.9), but output impedance will be low.

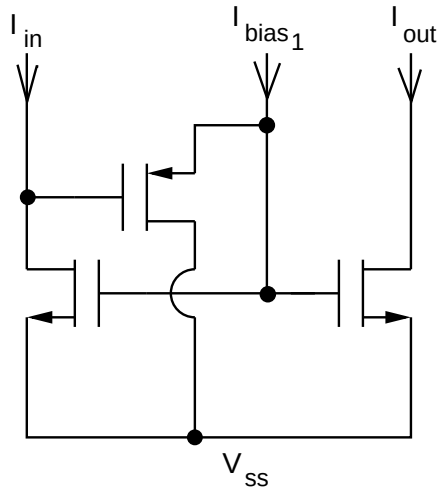


Figure A.10: Simple form of LVCM structure

A.6 Proposed Low Voltage DCC

LVCM needs less voltage across it to operate, one can use it to make other complex circuits work at low voltage. Here DCC is modified to a new circuit (LVDCC) for the low voltage application.

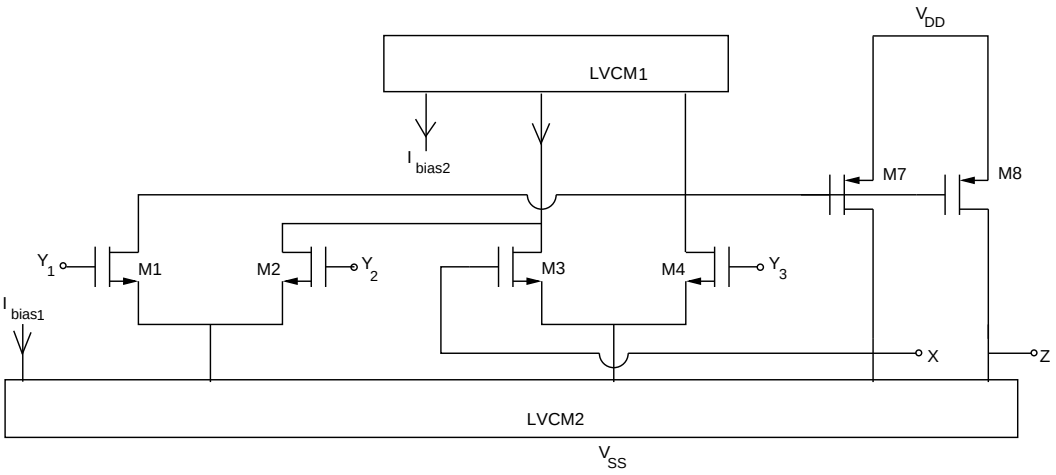


Figure A.11: Low voltage DCC structure

The circuit is shown in Figure A.11. Terminal behavior can be given as

$$V_x \approx [V_{y_1} - V_{y_2} + V_{y_3}] \tag{A.2}$$

A simplified circuit is shown in Figure A.12 using the simplified–LVCM (Figure A.10).

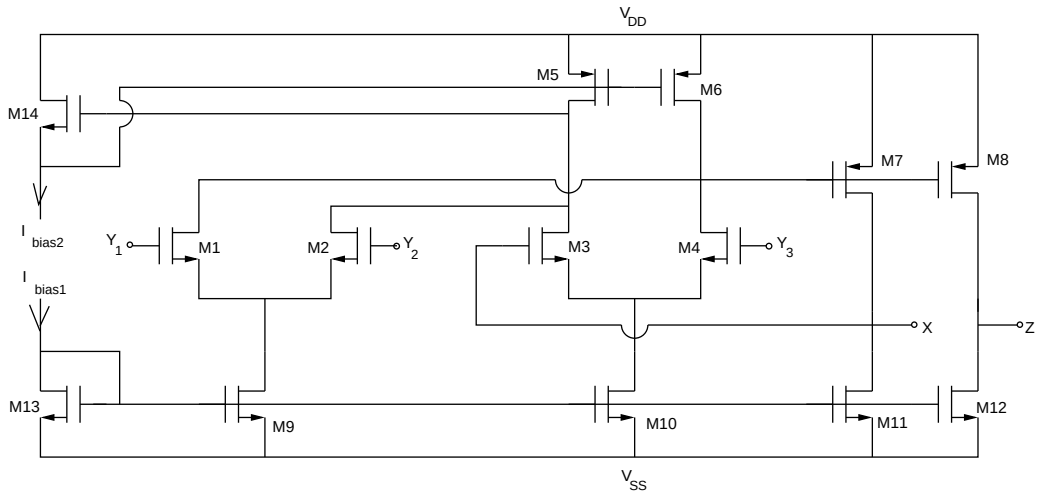


Figure A.12: Simplified circuit for low voltage DCC

(I_{bias1}) is bias current for the differential amplifier M1–M2 and M3–M4 and it is provided by M9 and M10. (I_{bias2}) is bias current for the LVCM.

M5, M6 and M14 forms simplified LVCM. M7, M11 and M8, M12 form the class–AB gain stage. Transistor M14 is biased such that it is in sub-threshold region, around nano–ampere order of current is pushed in to it (I_{bias_2}).

A.6.1 Analysis

To make the analysis simple, we have analyzed simplified LVDCC (Figure A.12). Here we have assumed unity gain for current mirrors, and perfect matching for transistors. However in practical realizations, several nonidealities must be present. The major factor we will consider here are finite transconductance g_m of the transistors, and transistor mismatch. The small signal analysis of the circuit will give relationship between V_{y_1}, V_{y_2}, V_{y_3} and V_x. For analysis, all transistors can be shown as their equivalent circuits. To simplify discussion, the body effect has been neglected and the two differential pairs are assumed to be identical. By solving node equations, we obtain

$$V_x \approx \frac{g_{m_7} g_{meq}}{g_{m_7} g_{meq} + (g_{d12} + g_{d34} + g_{d_6})(g_{d_7} + g_{d_I})}(V_{y_1} - V_{y_2} + V_{y_3})$$

with

$$g_{meq} = 2\frac{g_{m_1} g_{m_2}}{g_{m_1} + g_{m_2}} = 2\frac{g_{m_1} g_{m_2}}{g_{m_1} + g_{m_2}}$$

and

$$g_{dij} = 2\frac{g_{d_i} g_{d_j}}{g_{d_i} + g_{d_j}}$$

where g_{d_i} and g_{m_i} denote the drain conductance and transconductance of the transistor M_i, respectively, and g_{d_I} is the drain conductance of the current source. It is clear that voltage at port V_1, V_2 and V_3 will be accurately transferred to port X only if $g_{m_7} g_{meq} \gg (g_{d12} + g_{d34} + g_{d_6})(g_{d_7} + g_{d_I})$.

Similarly terminal impedance looking into X can be derived by setting V_{y_1}, V_{y_2} and V_{y_3} to zero, applying a test voltage V_x at node X and calculating the current I_x, the result is

$$R_x \approx \frac{(g_{m_3} + g_{m_4})(g_{d12} + g_{d34} + g_{d_6})}{2 g_{m_3} g_{m_4} g_{m_7}}$$

The terminal impedance at Z can also be derived as

$$R_z \approx \frac{1}{g_{d_8} + g_{d_I}}$$

For high frequency operation, the major limitation is due to the stray capacitance at terminal X. The high frequency response can be expressed in terms of V_{y_1}, V_{y_2}, V_{y_3} and V_x as

$$\frac{V_{x_1}}{V_{y_1} - V_{y_2} + V_{y_3}} \approx \frac{g_{m_7} g_{meq}}{(g_{m_7} - g_{meq} + g_{d_I})(\tau_1 s - 1)}$$

with

$$\tau_1 = \left[C_{gs_7} + C_{gs_8} + C_{gd_8}\left(1 + \frac{g_{m_8}}{g_{d_I} + g_{d_8}}\right) + 2C_{gd_6}\right]\left(\frac{1}{g_{d12} + g_{d34} + g_{d_6}}\right)$$

Where C_{gs_i} and C_{gd_i} are the gate–to–source capacitance and gate–to–drain capacitance of device M_i. respectively. The pole frequency is quite low and will be the dominant, frequency limiting factor of the circuit.

Differential voltage at input which is required to get zero voltage at terminal X (with respect to ground) is defined as the input offset voltage V_{os}. Large signal analysis is performed to solve the node equations. Then the offset voltage can be obtained as

$$V_{os} = (V_{T_2} - V_{T_1} + V_{T_3} - V_{T_4}) - \sqrt{\frac{I_d}{K_1 + K_2}}\left(\frac{K_2 - K_1}{K_2 + K_1}\right) - \sqrt{\frac{I_d}{K_3 + K_4}}\left(\frac{K_3 - K_4}{K_3 + K_4}\right)$$

Where K_i and V_{T_i} are the transconductance and the threshold voltage parameter of the device M_i, respectively.The first term is due to mismatch among the threshold voltages, which is bias–current independent and is a strong function of process cleanliness and uniformity. The second term is caused by geometrical mismatch and can be reduced by increasing W/L or reducing bias current.

A.6.2 Simulation Results

The circuit has been designed for minimum power dissipation and maximum range of voltage transfer with following parameters

- 0.18μm CMOS Technology
- $V_{DD} = +1.5V$
- $V_{SS} = -1.5V$
- $I_{bias_1} = 100\mu A$
- $I_{bias_2} = 2nA$

Transistor ratios are shown in Table A.1.

Transistors	**Type**	**W/L in μm/μm**
M1	NMOS	1.8/2.4
M2	NMOS	1.8/2.4
M3	NMOS	1.8/2.4
M4	NMOS	1.8/2.4
M5	PMOS	9.6/2.4
M6	PMOS	9.6/2.4
M7	PMOS	9.6/2.4
M8	PMOS	9.6/2.4
M9	NMOS	1.8/4.8
M10	NMOS	1.8/4.8
M11	NMOS	1.8/4.8
M12	NMOS	1.8/4.8
M13	NMOS	1.8/4.8
M14	NMOS	96/1.2

Table A.1: Transistor Ratios for low voltage DDCC

Simulation is carried out with the help of P-Spice for 1.2/mu technology with BSIM1 model. Voltage transfer characteristics is shown in Figure A.13. It transfers voltage nicely from -0.6volt to 1.4volts. For the input voltage between -1.5 to -0.6 Volts, the output voltage is V_{SS} because NMOS differential pair does not get enough V_{gs} for operation in this range. This problem is solved by using another differential made of PMOS (section–4.2.4).

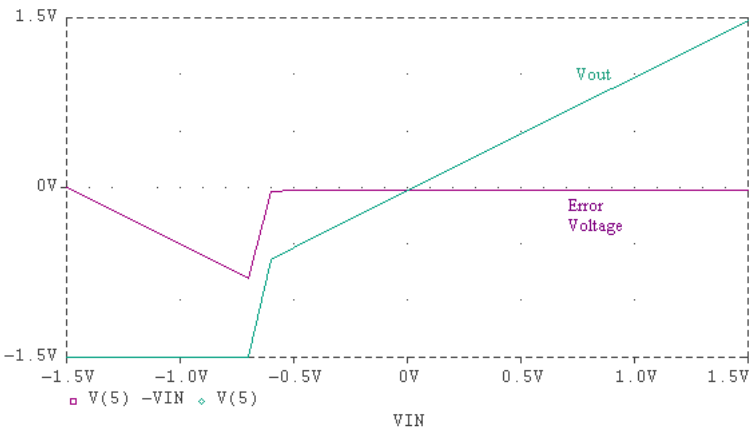


Figure A.13: Voltage transfer characteristics of low voltage DDCC

Current transfer characteristics is shown in Figure A.19, which shows it gives almost unity I_z/I_x current transfer ratio, and the current transfer is linear from X to Z node.

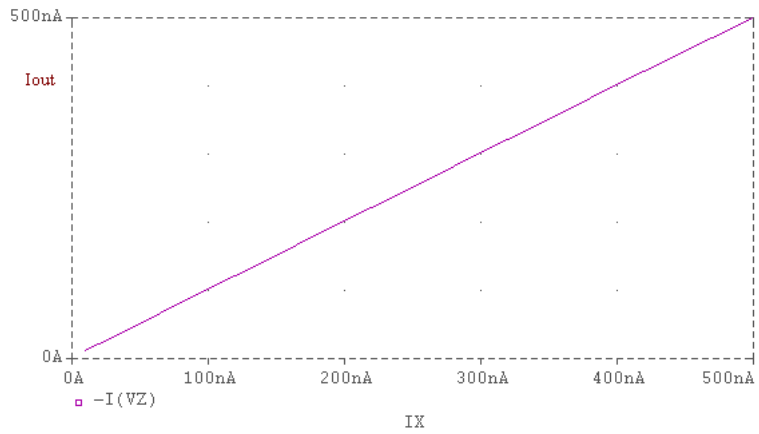


Figure A.14: Current transfer characteristics of low voltage DDCC

Frequency response for the output voltage is shown in Figure A.15. Which gives bandwidth of 12MHZ. Which is much more than DCC designed for ±3 Volts (12KHz).

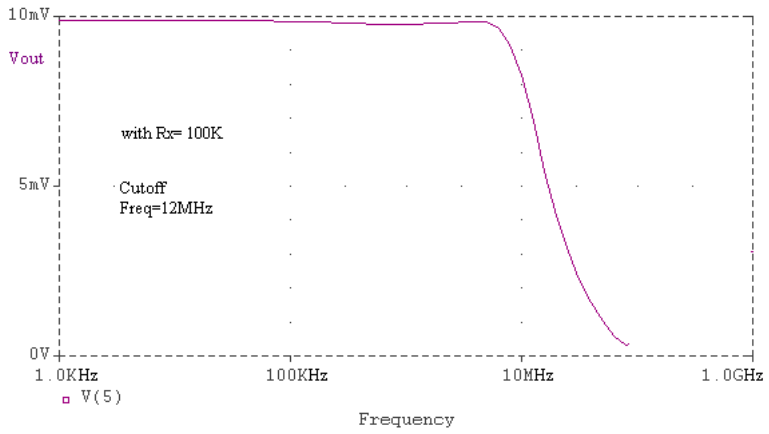


Figure A.15: Frequency response for output voltage

Frequency response for the output current is shown in Figure A.16. Which gives bandwidth of 15MHZ.

So using LVCM we can operate DCC up to supply of ±1.5 volts. Output swing of *proposed low voltage DCC* can be increased by reducing bias current but g_m will also decrease and the frequency response becomes poor . As output swing does not touch the supply, rail-to-rail technique can be used to increase the swing.

A.6.3 Rail-to-rail low voltage DCC

Output swing on the positive voltage side is good enough and very near (+1.4V) to positive supply (+1.5V). But in negative side it is quite low (-0.6V). When the output voltage goes for negative swing, after a limit, the NMOS differential pair does not get the sufficient gate-to-source voltage across it and hence it does not work. To increase the output range we can use

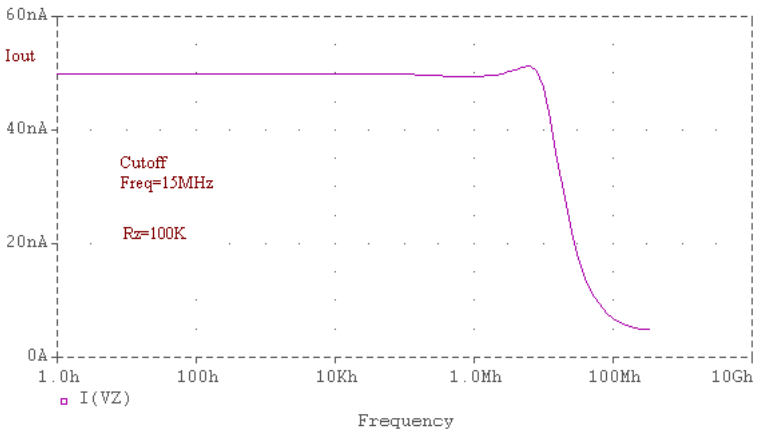


Figure A.16: Frequency response for output current

additional the PMOS differential pair for the negative swing. This technique has been reported for realization of universal current conveyor [95].The circuit for rail-to-rail, low voltage differential current conveyor is shown in Figure A.18.

M1 and M2 form the basic NMOS differential pair, and M3 and M4 form the PMOS differential pair for first section. Similarly in second section M5 and M6 is NMOS differential pair and M7 with M8 gives PMOS differential pair. LVCM and gain stage has been discussed earlier. For positive voltage swing NMOS pair will work and for negative swing PMOS pair will work. Its a constant g_m circuit, as it maintains g_m over the range. Transistor ratios for PMOS differential pairs are shown in Table A.2. And the output voltage characteristics is shown in Figure A.17. Output swing now becomes -1.3V to +1.4V which is almost rail-to-rail output.

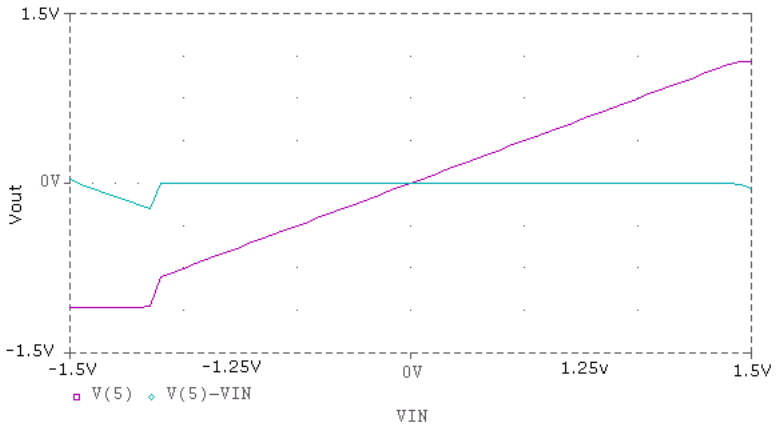


Figure A.17: Output voltage characteristics for rail to rail LVDCC

Transistors	**Type**	**W/L in μm/μm**
M1	NMOS	1.8/2.4
M2	NMOS	1.8/2.4
M3	NMOS	1.8/2.4
M4	NMOS	1.8/2.4
M15	NMOS	1.8/4.8
M16	NMOS	1.8/4.8
M17	NMOS	1.8/4.8
M18	NMOS	96/1.2

Table A.2: Transistor Ratios for rail-to-rail LVDCC

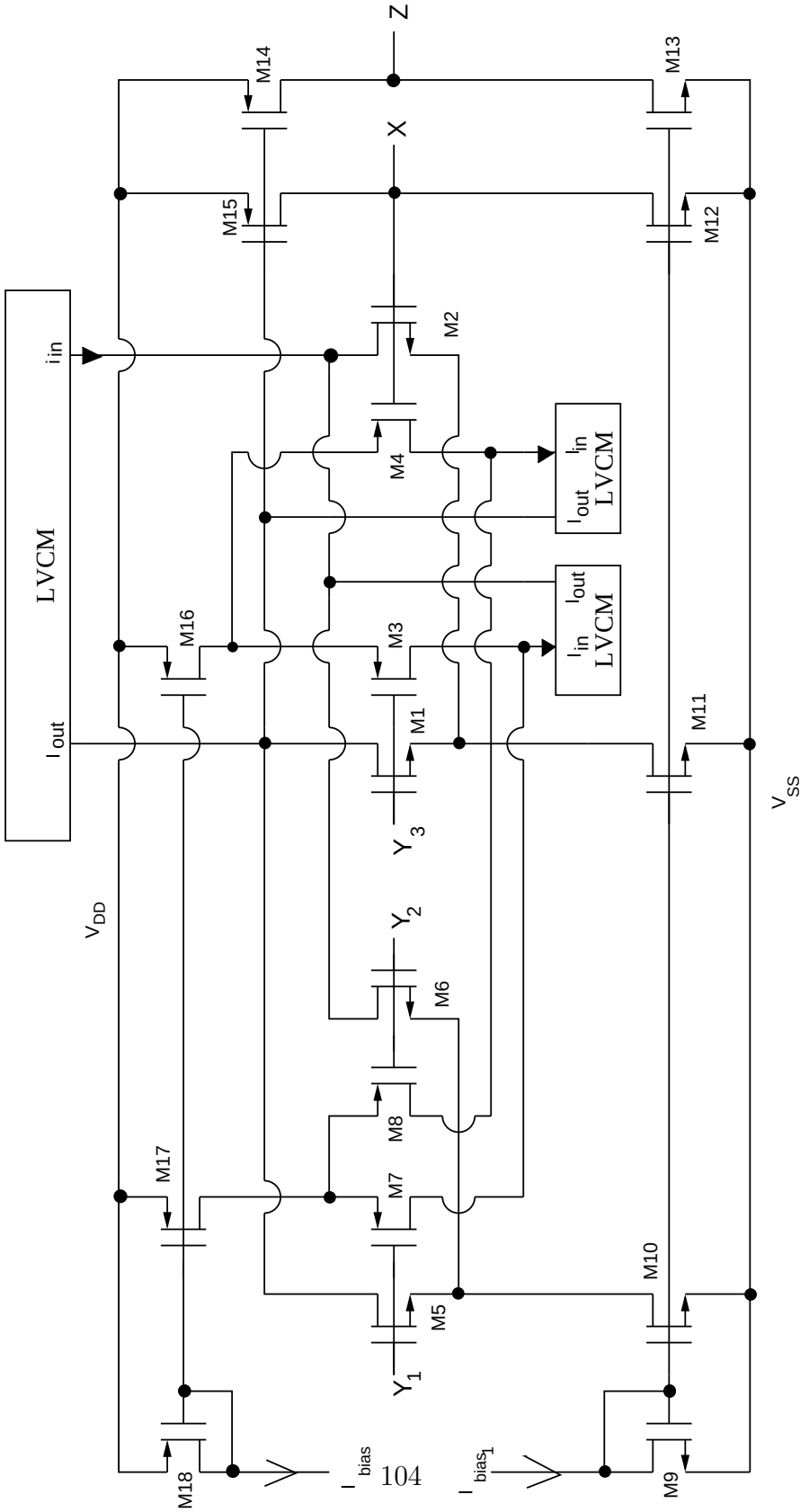


Figure A.18: Circuit for rail-to-rail LVDCC

A.6.4 Simulation Results

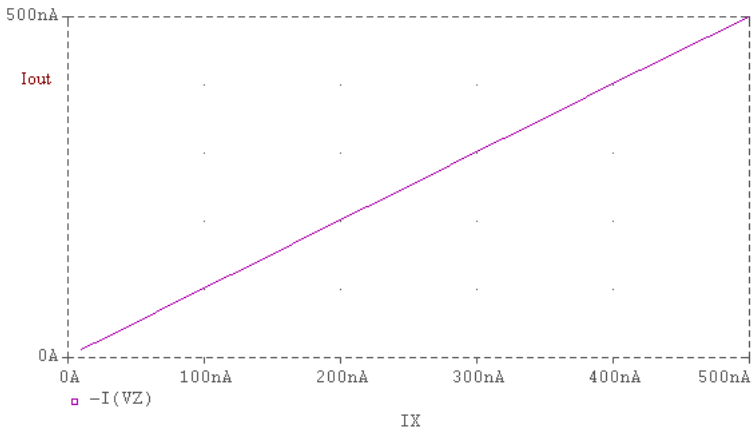


Figure A.19: Current transfer characteristics of low voltage DDCC

The design of proposed low voltage differential current conveyor is verified by simulations using 0.18μm CMOS technology. The circuit has been designed for minimum power dissipation and maximum range of voltage transfer. The supply voltage is $\pm$1.5V and I_{bias1} =100μA and I_{bias2} =2 nA. Voltage transfer characteristics from V_{in} to V_{out} is shown in Figure A.17. The horizontal line is the difference between V_{in} and V_{out}. It transfers voltage nicely from -1.3V to 1.4V and beyond that the M15 of Figure A.18 enters in to subthreshold region and behaves as mentioned in Section(3.5). Current transfer characteristics is shown in Figure A.19, which shows it gives almost unity current transfer ratio (I_z/I_x) and the transfer of current is linear from X to Z node.

A.6.5 LVDCC as Current Amplifier

So many applications for current conveyor have been listed in Section(3.3). The same proposed low voltage differential current conveyor design is configured as current amplifier for gain of 10 as shown in Figure A.20, with R_y =10k and R_x = 1k.

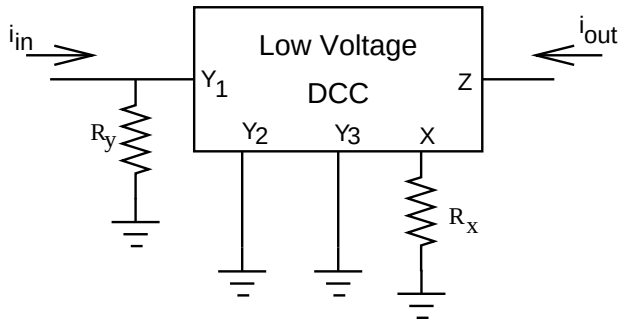


Figure A.20: Circuit for current amplifier

Terminal behavior as we know is

$$V_x = V_{y_1} - V_{y_2} + V_{y_3}$$

To avoid the complexity we have not used differential signal. So when Y_2 and Y_3 are grounded the relationship becomes

$$V_x = V_{y_1}$$

Input current is applied at the terminal Y_1 through a resistor R_y.

$$v_{y_1} = i_{in} R_y$$

$$i_x = \frac{v_x}{R_x} = \frac{v_{y_1}}{R_x}$$

$$i_{out} = i_z = i_x = \frac{V_{y_1}}{R_x} = \frac{i_{in} R_y}{R_x}$$

$$\text{gain} = \frac{i_{out}}{i_{in}} = \frac{R_y}{R_x}$$

It is simulated for $R_y = 10k$ and $R_x = 1k$ and seen that the gain is very near to the calculated one. The frequency response plot is shown in Figure A.21, which shows a bandwidth of 1.2MHz.

This idea can be extended to make a fully differential current conveyor (FDCC) also.

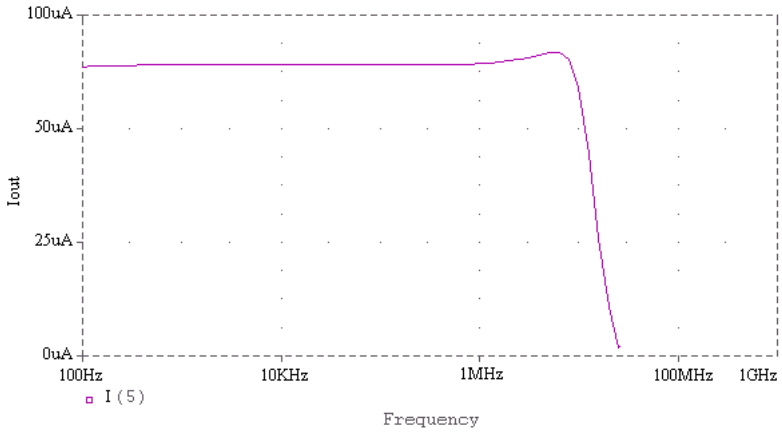


Figure A.21: Frequency response of current amplifier

Appendix B

Publication

B.1 Conferences

1. Sanjay K. Kasodniya, Dipankar Nagchoudhuri and N. M. Desai, "A New Low Voltage Differential Current Conveyor," in *IEEE/OSA/IAPR International Conference on Informatics, Electronics and Vision (ICIEV 2012)*, Dhaka, Bangladesh, May 18-19, 2012, pp. 837–841.

2. Sanjay K. Kasodniya, Biswajit Mishra and N. M. Desai, "Ultra Low Power Capacitive Power Management Unit in 0.18μm CMOS," in *IEEE International Conference on VLSI System, Architecture, Technology and Applicatons–VLSI-SATA 2016*, Benguluru, Jan. 11-12, 2016.

B.2 Journal (submitted for IET Circuit, Devices and System)

1. Sanjay K. Kasodniya, Munish Malik, Rahul Dhingani, H.N. Patel, H.S. Jatana, Guruvinder Singh, Biswajit Mishra, "Addressable Synchronous Asynchronous Differential Receiver Design in 0.18μm CMOS," *submitted for IET Circuit, Devices and System*

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