Design and Simulation of Single Electron Transistor Based High-Performance Computing System at Room Temperature

by

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Declaration

I hereby declare that

i) the thesis comprises of my original work towards the degree of Doctor of Philosophy in Information and Communication Technology at Dhirubhai Ambani Institute of Information and Communication Technology and has not been submitted elsewhere for a degree,

ii) due acknowledgment has been made in the text to all the reference material used.

Rashmit Patel

Certificate

This is to certify that the thesis work entitled Design and Simulation of Single Electron Transistor Based High-Performance Computing System at Room Temperature has been carried out by RASHMIT PATEL for the degree of Doctor of Philosophy in Information and Communication Technology at *Dhirubhai Ambani Institute of Information and Communication Technology* under our supervision.

Prof. Rutu Parekh	Prof. Yash Agrawal
Thesis Supervisor	Thesis Co-Supervisor

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Contents

Abstract

The VLSI technology has seamlessly grown over the years, that yields high-performance, low-power and high-density devices. Over the several decades, the performance of existing complementary metal-oxide semiconductor (CMOS) technology has been constantly improved by scaling of the transistors size. The scaling and heterogeneous 3D integration aids in achieving high-density logic. However, the performance of nanometer scale CMOS based designs is limited due to the short-channel effect, leakage current and process variations. There is a trade-off between speed and power consumption that significantly affects the performance of complex designs like computing devices. The nanoelectronics devices having the capabilities of heterogeneous 3D integration and functional integration with existing technologies serves potential solutions to future silicon technology challenges. These devices can overcome the aforesaid problems and escalates the capabilities of electronics devices in terms of speed, power, density, size and volume.

The single electron transistor (SET) is a promising and elegant nano-device which possesses several convincing features such as low energy consumption, efficient operational at room temperature, high switching speed, sustainable with scaling and reduced operating potentials to compete or outperform conventional CMOS technology. The SET can be used as basic element in either individual circuit or hybrid circuit with existing CMOS technology. The survey of individual SET based designs shows that these are at smaller block level with improper SET parameters, operating temperature, interconnect parasitics, etc. The bottleneck

with SET based designs having thousands of gates, is unavailability of either dedicated electronic design automation (EDA) tool or standard component library or synthesizer. This research gap is accomplished by proposed SET based computing system with consideration of realistic SET parameters and interconnects parasitics at room temperature operation.

The SET based computing system design is accomplished by utilizing industry standard Cadence Virtuoso analog design environment (ADE). It is carried out with gate level abstraction of SET Verilog-A behaviour model. The generated SET symbol is used to design basic combinational and sequential elements. The higher order circuit blocks of computing system are realized with these elements. Finally, a computing system is realized with integration of these foundation circuit blocks. The computing system is analyzed for a set of multiple instructions *i.e.* program level with the help of a developed tool.

The proposed design is carried out at transistor level abstraction. The formulated analytical model is performed for SET and it matches very closely with simulation model results. The each of the design block is verified for timing analysis. Also, the parametric analysis is compared with other research works. The proposed SET based computing system is considerably better with higher operating frequency (around 5 times), lower power dissipation (around 1.6 times) and higher execution of instruction per second (around 5 times) than its counterpart 16 nm CMOS technology. To check the robustness of the SET based computing system, variability analysis has been performed. It is observed that SET based computing system is less immune to supply voltage variations. This can be compensated by applying suitable voltage regulation techniques. On the other hand for temperature and process variations, it is envisaged that the SET based computing system is very robust. Hence, it is inferred that variability issues are very lesser in SET based systems and can be good alternative to replace conventional systems. Through the SET based design approach, integrated circuit can pack greater functionality with higher operating speed, smaller footprint, lower power consumption and lesser thermal budget.

List of Principal Symbols

ΔE	Change in energy measurement for time interval (Δt)
Δt	Time interval
C	Capacitance between terminals
C_{b}	Back gate capacitance
C_{d}	Tunnel junction capacitance at drain
C_{g}	Control gate capacitance
C_{j}	Tunnel junction capacitance
C_{s}	Tunnel junction capacitance at source
C_{Σ}	Total capacitance at the island
d	Drain
d_{g}	The separation between the island and gate
d_{i}	The separation between the island and the source or the drain
dq	Additional charge
e	Charge of an electron
E_{c}	Electrostatic charging energy
E_1	Initial electrostatic energy on the island
E_2	Electrostatic energy after one more electron on the island
$g1$	Control gate
$g2$	Tuning gate
h	Planck's constant
I	Single-electron tunneling current
I_{ds}	Drain to source current
k_{B}	Boltzmann's constant

n	Number of electrons
Q	Total charge
q	Charge on capacitor
R_{d}	Tunnel junction resistance at drain
R_{s}	Tunnel junction resistance at source
R_{t}	Tunnel junction resistor
s	Source
Si	Silicon
SiO_2	Silicon Dioxide
T	Operating temperature
t	Electrons localized time on the island
t_{g}	Thickness of the gate
t_{i}	Thickness of the tunnel junction
Ti	Titanium
U	Work done to add charge
V	Applied voltage
V_{bs}	Tuning gate to source voltage
V_{b}	External bias
V_{ds}	Drain to source voltage
V_{gs}	Control gate to source voltage
W_{g}	Width of the gate
W_{i}	Width of the tunnel junction

List of Abbreviations

3D	3-Dimentional
ADC	Analog-to-Digital Converter
ADE	Analog Design Environment
AFM	Atomic Force Microscopy
AL	Arithmetic-Logic
ALU	Arithmetic-Logic Unit
BCD	Binary-Coded Decimal
BEOL	Back-End-Of Line
CAD	Computer-Aided Design
CB	Coulomb Blockade
CISC	Complex Instruction Set Computer
CMOS	Complementary Metal-Oxide Semiconductor
CNT	Carbon Nano-Tube
DAC	Digital-to-Analog Converter
EDA	Electronic Design Automation
FET	Field Effect Transistor
GUI	Graphical User Interface
HDL	Hardware Description Language
I-MOS	Ionization MOSFET
IC	Integrated Circuit
ID	Instruction Decoder
IO	Input-Output
IPS	Instructions Per Second
IR	Instruction Register

ISA	Instruction Set Architecture
ITRS	International Technology Roadmap for Semiconductors
KOSEC	KOrea Single Electron Circuit
LSB	Least Significant Bit
MAR	Memory Access Register
MIB	Mahapatra–Ionescu–Banerjee
MIPS	Millions of Instructions Per Second
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MSB	Most Significant Bit
NEMS	Nano Electro-Mechanical Systems
NSET	N-type SET / Pull-down SET
PC	Program Counter
PLA	Programmable Logic Array
PSET	P-type SET / Pull-up SET
PVT	Process-Voltage-Temperature
QD	Quantum Dot
RF	Radio Frequency
RISC	Reduced Instruction Set Computer
RTL	Register Transfer Level
SENECA	Single Electron NanoElectronic Circuit Analyzer
SET	Single Electron Transistor
SIMON	SIMulation Of Nanostructures
SiNWs	Si Nano-Wires
SOI	Silicon-On-Insulator
SPICE	Simulation Program for Integrated Circuit Emphasis
SRAM	Static Random Access Memory
TFET	Tunnel FET
VHDL	VHSIC Hardware Description Language
VHSIC	Very High Speed Integrated Circuit
VLSI	Very Large-Scale Integration

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CHAPTER 1

Introduction

1.1 Future trends in microelectronics and nanoelectronics

An historical observation by Gordon Moore says that the market demand (and semiconductor industry response) for functionality per chip (bits, transistors) doubles every 1.5 to 2 years [1, 2]. The "Moore's Law" depicts a consistent macro trend and key indicator of successful leading-edge semiconductor products. The metal oxide semiconductor field effect transistor (MOSFET) transistor has gone through scaling for the last several years, and drive the complementary metal-oxide semiconductor (CMOS) technology towards the deep sub nano-meter regime. According to international technology road-map for semiconductors (ITRS) [1], the integrated circuit (IC) will be fabricated with sub nanometer range and, beyond that the quantum mechanical effects become predominant. It implies that the shrinkage of further MOSFET dimensions are unfeasible. In the concept of miniaturization of devices, physicist Richard challenges the miniaturization and focuses on the idea of how to manipulate and control the matter in atomic and molecular levels [3]. In 1991, Sumio Ijima discovered the carbon nano-tube (CNT) at the NEC laboratory, Tsukuba, Japan [4]. This discovery has become the milestone of today's nanoscience and nanotechnology. It motivated scientists, engineers, researchers, and technologists to investigate on materials at nanometer scale. Fig. 1.1 shows the direction for research in future of ICs development. The three main domains are (1) More Moore, (2) More than Moore, and (3) Beyond CMOS. Moore's law

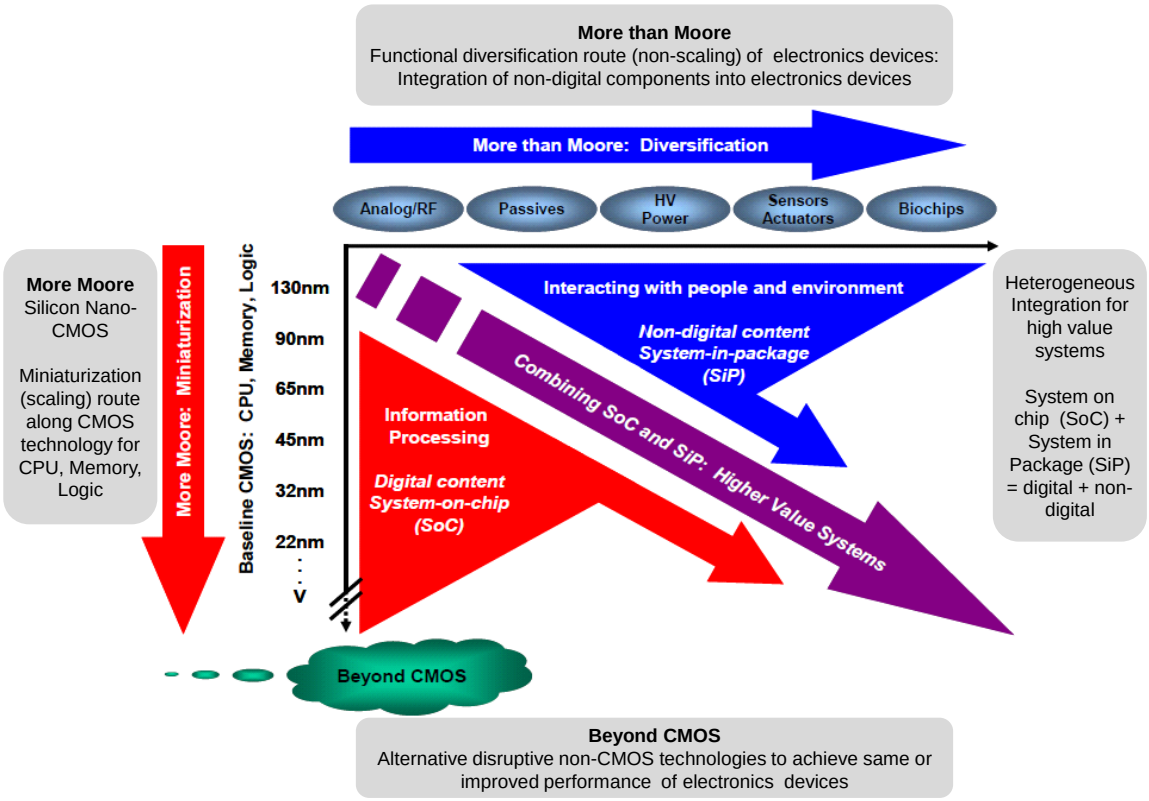


Figure 1.1: Nanoelectronics technology development paths [1].

is applicable to (1) only, whereas (2) and (3) does not support aggressive scaling. "More Moore" provides CMOS miniaturization for higher performance and lesser power at lower cost. The second trend "More than Moore" guides compact systems by heterogeneous integration of digital and non-digital functionalities. "Beyond CMOS" is mainly non-Si CMOS devices which have the capability to scale the performance of IC beyond the ones attained by ultimately scaled CMOS.

The prime goal of IC design is to achieve low power and small delay in logic and memory devices with minimal footprint. Scaling of technology plays an important role for performance improvement in terms of signal integrity, delay and power dissipation. However, continuous scaling of MOSFET devices below tens of nanometer dimensions causes several non-ideal issues like short channel effect, power dissipation, leakage current, and process variation [5–7]. These issues can be overcome by the usage of novel nano-electronics devices and, the future trend towards to IC development belongs to heterogeneous 3D integration of different technologies [8]. Nano-electronics typically cover electronics devices

and technology in which the critical dimensions are less than 100 nm. Because of nano-scale dimensions, these devices exhibit distinct electrical, optical or mechanical properties that encourage the discovery of new area for information processing. It brings out the engineering aspects to produce such components at micro or nano level for various applications. The ITRS road map shows the future of integrated circuits lies in nano-devices.

ITRS organizes emerging nano devices into 3 categories as described in Table 1.1 [1, 9]. The category-1 (Extending the channel of MOSFETs) lists MOSFET structures that use alternate channel material. The devices mentioned under this category offers a higher quasi-ballistic charge carrier velocity and higher mobility than strained silicon or different geometry with parameters relevant to high and general performance logic. The category-2 (Unconventional FETS, Charge-based Extended CMOS Devices) offers hybrid integration with existing CMOS technology to extend the functionality of ultimately scaled CMOS. The devices like, the tunnel FET (TFET), impact ionization MOSFET (I-MOS), negative gate capacitance (Cg) MOSFET, single electron transistor (SET) etc. offers lower power dissipation by providing a steeper sub threshold turn-on current voltage characteristic. The category-3 (beyond CMOS devices) lists the novel devices for more specialized tasks like associative processing, communication, multi-valued

Table 1.1: Emerging nanodevices

Category 1 MOSFETs, Extending the channel of MOSFETs to the End of the Road-map	**Category 2 Unconventional FETS, Charge-based Extended CMOS Devices**	**Category 3 Non-FET, Non Charge-based 'Beyond CMOS' Devices**
CNT FETs Graphene nanoribbons III-V Channel MOSFETs Ge Channel MOSFETs Nanowire FETs Non-conventional Geometry Devices	Tunnel FET I-MOS Spin FET SET NEMS switch Negative Cg MOSFET Excitonic FET Mott FET	Collective Magnetic Devices Spin Transfer Torque Logic Moving domain wall devices Pseudo-spintronic Devices Nanomagnetic (M:QCA) Molecular Switch Atomic Switch

logic and ferromagnetic elements for non-volatility, radiation hardness and error tolerance. The usage of nano devices has emerged as one of the key technologies in the quest to establish a sustainable energy system in miniaturized footprint. The final outcome at nano-scale devices is the development of quantum dot (QD). It is a nano particle having the dimensions reduced to below 100 nm, that is the main building block of SET.

The SET is a potential nano-scale device that works on quantum mechanical principle and can be co-integrated to widely adopted CMOS technology to enhance performance of scaled CMOS [9]. The first step in the applications of circuit is to integrate SET with CMOS technology using back-end-of line (BEOL) fabrication method where in SET circuits address low power modules for logic and memory operations. Hence, in order to interface with nano-CMOS, it is desirable to operate SET circuits at nano-CMOS compatible operating voltage (0.8 V) for input-output (IO) and signal restoration. In the second phase, there is need of programmable design using standalone SET technology for room temperature operation.

1.2 Single electron transistor

SET technology have been widely studied because of their unique multi-functionality with ultra-low power dissipation and scalability down to the sub-nanometer regime. The SET device structure is similar to MOSFET which helps in each and every aspect of design. The work done in the field of SET has been surveyed in respect to SET fabrication, modeling, and design. These have been meticulously explored by referring several books, book chapters, journals, conferences, and symposiums which have been discussed in next chapter.

The research work related to SET fabrication shows that it is practical and feasible to fabricate SET. Also, monolithic fabrication of SET with CMOS technology complements the conventional Si-CMOS performance. With the latest fabrication technology, it is viable to fabricate sub atto-farad range of SET capacitance which enables its operation at room temperature. Several SET modeling approaches have been compared in the aspects of tool integration facility, parameter modifications and comparatively faster simulation. Initially,

considering lower driving capability of SET, several hybrid SET-MOSFET based logic circuits have been proposed and analyzed [10]. However, these have practical limitations of fabrication on the same chip and large number of transistors and henceforth, power dissipation. So, only SET based circuits have been investigated and proposed by several researchers. From these works, it is inferred that design with only SET is effective in attaining faster operation with lower power dissipation. The SET and 22 nm CMOS cascaded inverter results for bandwidth, power and delay are reported in [11]. It shows that with SET device, power, bandwidth and delay are 4 nW, 210 GHz and 3.1 ps respectively. On the counterpart with the 22 nm CMOS technology, these values are 130 nW, 81 GHz and 7.8 ps respectively. The effective area occupied by MOS transistor and SET at 22 nm technology node are 26620 nm^2 (using minimum λ rules [12]) and 16324 nm^2 [13] respectively. These clearly indicate SET advantages over 22 nm CMOS technology. Also, the metallic SET fabricated with BEOL process can be easily stacked above the CMOS platform to realize 3D integrated circuits for higher-volume and lesser-footprint. Using SET various designs have been carried out for analog, digital, radio frequency (RF), sensor applications etc. with its multi-gate and multi-bit characteristics. The SET based design in digital domain reveals up to small logic block level designs. The complete complex system design such as computing system using SET that can work at room temperature has not been implemented to the date and best of our knowledge. To fill up this research gap and highly needed research in this area, we have designed a SET based computing system with incorporation of realistic SET parameters and interconnect parasitics using Cadence Virtuoso tool set.

1.3 High performance computing system

Computing system is a general purpose device to receive, process, manage and present data. It comprises of hardware and software support for user intervene. The computer hardware consists of various design blocks like arithmetic-logic unit (ALU), memory, controller, registers, etc [14]. The computer software is a program which gets executed on computer hardware. The program comprises of set of user defined instructions. The basic requirements for computing system are higher speed, smaller size, lower power consumption, versatility and

reliability. The computing systems are more commonly referred as microprocessors. There are basically two kinds of microprocessors namely complex instruction set computer (CISC) microprocessor and reduced instruction set computer (RISC) microprocessor.

The major issue in microprocessor design is significant increase of the power consumption because of to high speed operation [15, 16]. The GHz operating range and increase in number of transistors escalate overall switching power. The transition activity causes charging and discharging of internal node capacitances that leads to increase in the dynamic power dissipation. The commercially available microprocessors have transistor size in nanometers. Due to thin insulating layers, these are prone to current leakage and hence static power dissipation increases. Because of these, the management of chip temperature and heat dissipation become critical. The reduced transistor size alleviates problems in complex manufacture process. The reduction in power, area and the improvement of speed require optimization at all design aspects. These factors implies the perturbance in Moore's law and demands for other ways to improve performance of computing systems.

1.4 Open questions and project objectives

The previous research works show that the future silicon technology challenges are limited by increased power dissipation and thermal heating due to continuous scaling. Future silicon technology challenges can be reduced by the heterogeneous 3D integration of various technologies and integration of various circuit blocks like memory elements, processors and interconnects. With the latest fabrication technology, it is viable to fabricate sub atto-farad range of SET capacitance which enables its operation at room temperature, lower delay, lesser power and higher density. These fulfill basic necessity of very large-scale integration (VLSI) design. Various designs have been carried out using SET-MOS hybrid and only SET based technologies. It is investigated that, these designs are at relatively individual logic blocks with very few number of transistors. The designs work at either lower temp range or considers unrealistic parameters or negligence of interconnect

parasitic, etc. However, complex and large circuit designs such as microprocessors or computing systems have not been yet implemented and explored.

Objective

To fill up this research gap and highly needed research in this area, a computing system is realized with incorporation of realistic SET parameters for room temperature operation and interconnect parasitics. Also, the design is compatible for heterogeneous integration over existing CMOS technology. In order to achieve the SET based stand-alone computing system design, the research objectives are framed as:

1. Exploration of SET device for VLSI circuits and system design.
2. Design and implementation of SET based computing system with incorporation of realistic SET parameters and interconnects at room temperature operation.
3. Tool development for implementation and verification of SET based computing system.
4. Performance comparison of SET with conventional 16 nm CMOS technologies based computing systems.
5. Process-voltage-temperature (PVT) variation analysis of SET based computing system.

1.5 Thesis frame work

This thesis presents a detailed design of SET based computing system and its brief frame work is described herewith:

Chapter-2 shows background work for proposed SET based computing system. The aspects of SET theory, fabrication, modeling and designs are discussed in this chapter. It begins with, the basic theory of SET using tunneling phenomena and electron transport based on free electron model. Various fabrication and modeling methods are discussed thereafter. The hybrid SET-MOS and only SET based designs are reviewed and detailed. In the next part, theoretical aspect of computing system is discussed. This section describes the computing system architecture, details of their features and instruction execution.

Chapter-3 describes the detailed design of SET based computing system. The proposed SET based computing system employs the von-Neumann architecture where the instructions and data share the same memory. It is designed with bottom-up approach where the design is realized from basic combinational and sequential elements. Various SET based higher order blocks like ALU, controller, static random access memory (SRAM) are detailed thereafter. The SET based computing system realization using integration of necessary blocks are shown at the last. The detailed timing analysis is shown along with the design description.

Chapter-4 discusses the verification aspect and tool design for SET based computing system. The computing system design needs complex stimuli set for its verification that is not optimum with traditional individual sources simulations and can be accomplished by a vector file. But, for a large design like computing system, it is advisable to generate though automated tool instead of defining it manually. The necessity of the tool, its architecture and tool code executions are detailed in this chapter. The result of computing system verification using the vector file generated from the developed tool are shown at the last.

Chapter-5 describes the results and analyses of proposed SET based design blocks and computing system. The modeling aspects of pull-up SET (PSET) and pull-down SET (NSET) are described in the beginning. Thereafter, parametric analytical results of individual SET based design block are discussed. The results of proposed SET based design blocks are compared with previous research work. Further, the performance comparison of SET and 16 nm CMOS based computing system is investigated. At last, results of PVT variation analyses for SET based computing system are presented.

Chapter-6 shows the conclusion on the proposed work. The conclusion summaries design, results and various analyses of proposed work. Finally, it is revealed that the SET performs considerably better with higher operating frequency (around 5 times), lower power dissipation (around 1.6 times) and higher execution of instruction per second (around 5 times) than its counterpart 16 nm CMOS technology.

CHAPTER 2

Background of SET Based Computing System

The proposed work carries out design, verification and analyses for a SET based computing system. The theoretical aspects of proposed work are divided in two sections, 1) SET theory and 2) computing system theory. Sections 2.1–2.4 describe SET theory on its operation, free electron transport, fabrication, modeling and designs. Section 2.5 describes basic theory of generalized computing system, architecture, instruction execution and overview of its design.

2.1 SET Theory

The conventional MOSFET operates by virtue of charge flow between drain and source terminals which is controlled by gate voltage. The millions of electrons flowing through the channel during current conduction leads to heat dissipation and loss of power, which is undesirable. The SET is a similar device to MOSFET except for the conducting channel [10, 17]. The island or QD of SET separates the source and drain, that replace the conventional MOSFET channel and controls the electron tunneling. In SET, there is no channel and reverse-bias junctions, hence there is no sub-threshold and reverse-bias junction leakage currents. The island separates both the source and drain terminals by ultra-thin dielectric insulator and forms tunnel junctions. The SET operates by electron tunnel through two junctions in two steps *i.e.* from source to island and from island to drain. The article [18] consolidates the working principle of SET and compares its performance with existing conventional field effect transistor (FET) technology. It highlights benefits, limitations and applications of the two aforemost said technologies. SET theory,

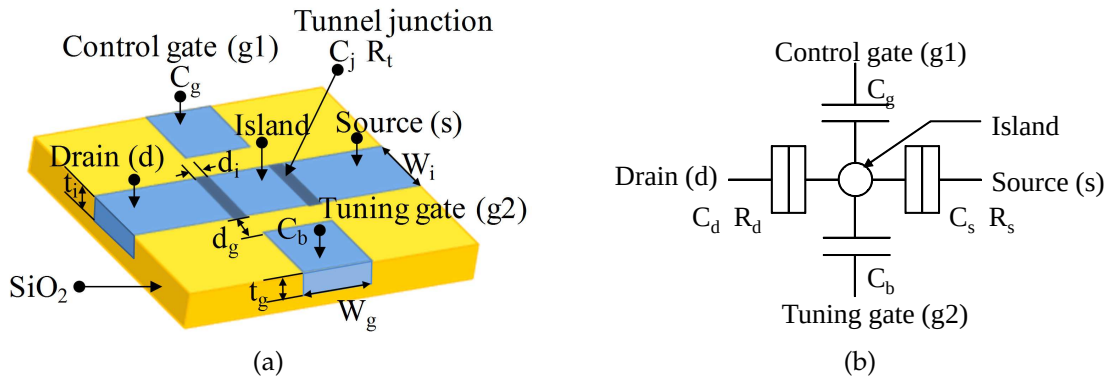


Figure 2.1: SET. (a) 3D structure. (b) Equivalent model and its associated parameters with each of the terminals.

working principle, analyses, fabrication and simulation have been presented in [19]. The physical structure of dual gate SET having four terminals namely source (s), drain (d), control gate (g1) and tuning gate (g2) is shown in Fig. 2.1(a). The tuning gate of SET is also referred as back gate. The C_g and C_b are the gate capacitance at control gate (g1) and back gate (g2) respectively. Each of the tunnel junction has associated parameters as junction capacitance (C_j) and junction resistance (R_t). The SET device physical dimensions considered in the present work are shown in Fig. 2.1(a) and listed in Table 2.1. The physical dimensions and parameters are considered from [9]. The physical dimensions W_i, d_i, t_i, W_g, d_g and t_g refers as width of the tunnel junction, the separation between the island and the source or the drain, thickness of the tunnel junction, width of the gate, separation between the island and gate, and thickness of the gate respectively. Based on these physical parameters the electrical parameters are derived and described in Section 3.1.3.

Table 2.1: SET physical dimensions

W_i (nm)	d_i (nm)	t_i (nm)	W_g (nm)	d_g (nm)	t_g (nm)
3 - 20	2 -8	1 -10	30	20 -60	1 -10

Fig. 2.1(b) shows the generalized equivalent model for computer-aided design (CAD) framework. It shows relevant SET parameters like control gate capacitance (C_g), tuning gate capacitance (C_b), junction capacitance at source (C_s), junction capacitance at drain (C_d), tunnel resistance at source (R_s) and tunnel resistance at drain (R_d). The proposed work uses a SET with dual gate to have the designs

similar to conventional CMOS based designs. The tunnel junctions can be treated as leaky capacitor as electrons tunnel through it. The potential of island is controlled by gate terminal(s) which is separated by thick dielectric.

The basic theory of SET can be described by capacitor charge and associated equations. A capacitor consists of two parallel conductive plates (usually a metal) which are separated by the dielectric. On supplying a voltage across these plates, the current flows though it which generates positive charge on one plate and an equal negative charge on the other plate. The electrostatic capacitive charge can be given as,

$$q = C\,V \tag{2.1}$$

Here, C is the capacitance between terminals and V is the applied voltage. Transporting additional charge (dq) to other plate of a capacitor requires work done (U) against applied voltage (V). It is given by,

$$\begin{aligned} U &= \int V\,dq \\ &= \int \frac{q}{C}\,dq \end{aligned} \tag{2.2}$$

For the total charge (Q), the work performed can be determined as,

$$\begin{aligned} U &= \frac{1}{C}\int_0^Q q\,dq \\ &= \frac{Q^2}{2C} \end{aligned} \tag{2.3}$$

For SET, the work done (U) for charge transfer is referred as the electrostatic charging energy (E_c) and given by $Q^2/2C_\Sigma$ (Eq. 2.3). Here, the Q is the charge on the island and C_Σ is the total capacitance of the island. The C_Σ is summation of capacitance from source to island, drain to island and gate to island.

For tunneling of an electron (charge) to the island, there is need to determine appropriate conditions. Let us say, there are fixed numbers of electrons that exists on the island and having initial electrostatic energy (E_1) which is $Q^2/2C_\Sigma$.

Considering the one additional electron on the island, the electrostatic energy (E_2) on island will be $(Q-e)^2/2C_\Sigma$. That gives,

$$E_1 > E_2$$

$$E_1 - E_2 > 0$$

$$\frac{Q^2}{2C_\Sigma} - \frac{(Q-e)^2}{2C_\Sigma} > 0$$

$$\frac{Q^2 - (Q-e)^2}{2C_\Sigma} > 0$$

$$(Q-(Q-e))(Q+(Q-e)) > 0$$

$$e(2Q-e) > 0$$

$$Q > e/2 \tag{2.4}$$

For SET, $Q = |V|C_\Sigma$ where $|V|$ is the voltage drop across tunnel junction. So, the Eq. 2.4 can be derived further to,

$$\mid V \mid C_\Sigma > e/2$$

$$\mid V \mid > e/2C_\Sigma \tag{2.5}$$

Eq. 2.5 in principle defines the condition for electron transfer and when this condition is not satisfied the electron can not tunnel. An electron tunneling is valid when the electrons are well localized in the island. The concept of localization is quite evident in classical mechanics, where one electron is either there or not. However, in quantum mechanics it is uncertain. According to Heisenberg's energy uncertainty (ΔE) principle, $\Delta E \Delta t > h$ (where h is Planck's constant). Now in order to make the electrons localized on the island for the time t must be much greater than Δt. That is,

$$t \gg \Delta t$$

$$t \gg h/\Delta E \tag{2.6}$$

Now, the current (I) can be described by e/t for single-electron tunneling, and the $\Delta E < eV_\mathrm{b}$ (where V_b is the external bias). Therefore, inserting $t = e/I$ and

$\Delta E = eV_{\mathrm{b}}$ in Eq. 2.6 gives tunnel resistor (R_{t}) requirements. It is described as,

$$
\begin{aligned}
&e/I \gg h/eV_b \\
&V_b/I \gg h/e^2 \\
&R_t \gg h/e^2 \\
&R_t \gg 25.8\,k\Omega
\end{aligned}
\tag{2.7}
$$

For single-electron devices, the thermal energy should not allow an electron to tunnel onto the island. The E_{c} must be greater than thermal energy which forces electron tunneling by E_{c} only. It is given by,

$$
\begin{aligned}
&E_c \gg k_B T \\
&e^2/2C_\Sigma \gg k_B T
\end{aligned}
\tag{2.8}
$$

Here, k_{B} is Boltzmann's constant and T is the operating temperature. From eq. 2.8, it is derived that $T \ll e^2/2k_{\mathrm{B}}C_\Sigma$.

The working of SET can be described by Coulomb blockade (CB) and quantum tunneling [10, 17]. To understand its working operation, the source and the drain terminals are grounded whereas the gate is biased with a gate voltage V_{g}. It results, total charge of $\Sigma C_{\mathrm{g}} V_{\mathrm{g}}$ at the gate. If the total charge of $-ne$ (where, n and e are number and charge on electron respectively) on the island is stabled with that in the gate, then $\Sigma C_{\mathrm{g}} V_{\mathrm{g}} = ne$ is satisfied. In this condition, since the number of electrons, n is stable, no current flows through the island. This is known as the Coulomb blockade condition. Further increase in the gate voltage, increases total charge on the gates and the charges become unbalanced. With $\Sigma C_{\mathrm{g}} V_{\mathrm{g}} = (n + 1/2)e$, the electrostatic potential for n electrons and $n + 1$ electrons becomes equal, which implies n or $n + 1$ electrons in the island. When a small voltage is applied between the source and drain electrodes, electrons flow from the source to the island leaving $n + 1$ electrons in the island. The number of electrons in the island returns to n, once an electron has tunnelled from the island to the drain. The current hence flows due to single electron tunneling by repeating these steps.

The SET electron transport and CB conditions are described in Figs. 2.2 – 2.11. The source terminal is grounded and shown with preliminary source of electrons. The drain terminal is connected to supply voltage V_{ds} at $e/2C_\Sigma$ (2.5). Here, $e/2C_\Sigma$ is equal to and mentioned as 'a' . Also, the representation of 'a' along with its multiple values '2a', '3a', '4a' and '-a' are shown in Figs. 2.2 – 2.11. The island potential is controlled by gate voltage (V_{gs}). The vertical lines represent the potential at drain, island, and source terminals. The horizontal red lines represent the voltage at respective terminals. The SET tunneling is described for four different operating conditions which are,

i When the island potential is less than $e/2C_\Sigma$ (Fig. 2.2)

ii When island potential is between $e/2C_\Sigma$ and $2e/2C_\Sigma = (e/C_\Sigma)$ (Figs. 2.3 – 2.5)

iii When island potential is between e/C_Σ and $3e/2C_\Sigma$, (Figs. 2.6 – 2.7) and

iv When island potential is between $3e/2C_\Sigma$ and $4e/2C_\Sigma = (2e/C_\Sigma)$ (Figs. 2.8 – 2.11)

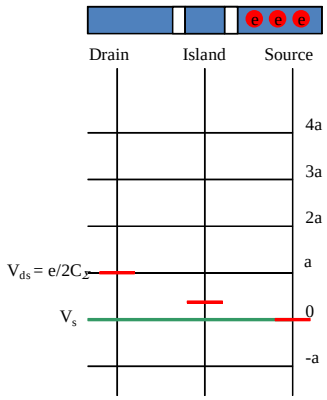


Figure 2.2: The island potential is less than $e/2C_\Sigma$.

Fig. 2.2 shows the condition when the island potential is less than $e/2C_\Sigma$. Here, the potential difference between source to island and island to drain is less than $e/2C_\Sigma$. As a result, the electron transfer does not take place. This condition where electron transport is blocked is referred as Coulomb blockade.

By increasing voltage at gate (V_{gs}), the potential to island is increased which is depicted by a black arrow in Fig. 2.3. Now, the source to island potential is greater than $e/2C_\Sigma$. This condition justifies the condition for an electron transfer. This condition is also valid for the initial island potential between $e/2C_\Sigma$ and $2e/2C_\Sigma = (e/C_\Sigma)$.

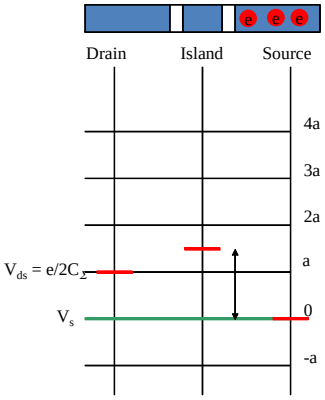


Figure 2.3: The island potential is between e/C_Σ and $e/2C_\Sigma$.

In continuation to Fig. 2.3, the island has one electron transported from source. This condition is shown in Fig. 2.4. Due to an electron, the potential of island is dropped by e/C_Σ is depicted by a black arrow. Now, the potential difference between island and drain is greater than $e/2C_\Sigma$.

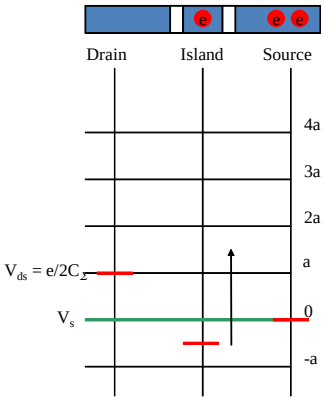


Figure 2.4: An electron transfer condition for Fig. 2.3.

In continuation to Fig. 2.4, an electron will move from island to drain that restores island potential to the value as per Fig. 2.3. The processes from Fig. 2.3 to Fig. 2.5 will repeated continuously and current path is established from source-island-drain.

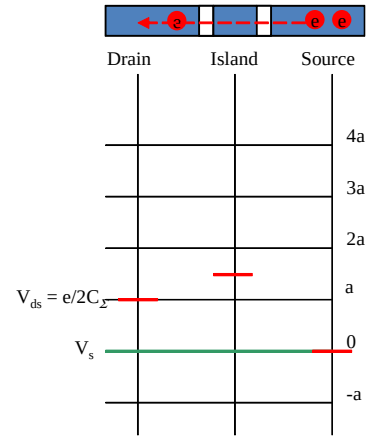


Figure 2.5: Current flow path establishment for Fig. 2.3.

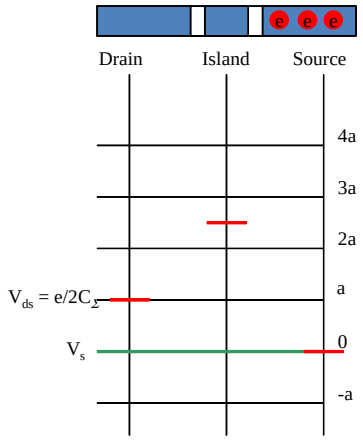


Figure 2.6: The island potential is between e/C_Σ and $3e/2C_\Sigma$.

Fig. 2.6 shows the condition where the island potential is between e/C_Σ and $3e/2C_\Sigma$.

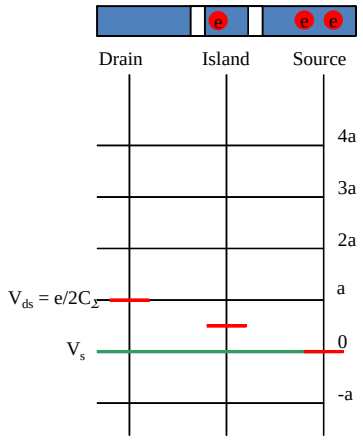


Figure 2.7: The island potential bring down condition for Fig. 2.6.

In continuation to Fig. 2.6, due to enough potential difference between source and island, an electron is transported from source to island. It is shown in Fig. 2.7. As stated above, due to an additional electron the potential at island is reduced by e/C_Σ. But, the potential difference between island and drain is less than $e/2C_\Sigma$. So, the electron cannot be transferred from island to drain. This condition is again CB with one additional electron at island.

Due to further increase of voltage at gate (V_{gs}), the island potential is more than $3e/2C_\Sigma$. Fig. 2.8 shows this condition that refers the island potential is between $3e/2C_\Sigma$ and $4e/2C_\Sigma$.

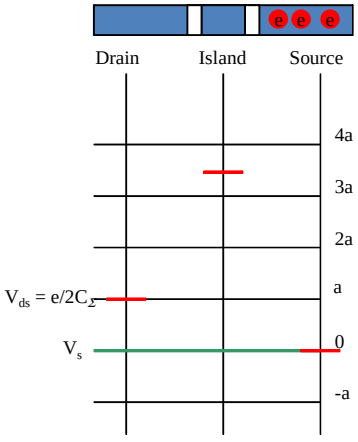


Figure 2.8: The island potential is between $3e/2C_\Sigma$ and $4e/2C_\Sigma$.

Due to enough potential difference between source and island, an electron is transported from source to island which is shown in Fig. 2.9. As stated above, due to an additional electron the potential at island is reduced by e/C_Σ. Also, the island potential after electron transfer is further higher than $e/2C_\Sigma$.

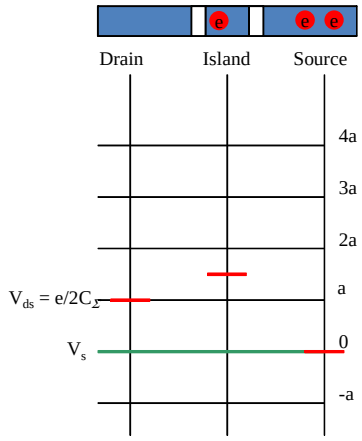


Figure 2.9: The island potential bring down for Fig. 2.8.

In continuation to Fig. 2.9, due to potential difference between source and island, one more electron is transferred from source to island and island potential is further reduced by e/C_Σ. This condition is shown in Fig. 2.10

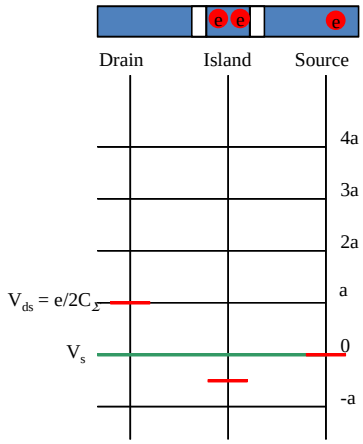


Figure 2.10: The island potential further bring down for Fig. 2.9.

In continuation to Fig. 2.10, as the island potential is reduced below $e/2C_\Sigma$, an electron is transferred from island to drain and again the island potential restores to as Fig. 2.9. So, this case (from Fig. 2.9 to Fig. 2.11) is the same as the Fig. 2.3 to Fig. 2.5 with an extra electron. Here, the current path is established from source-island-drain with residue of an extra electron at island. This condition is shown in Fig. 2.11.

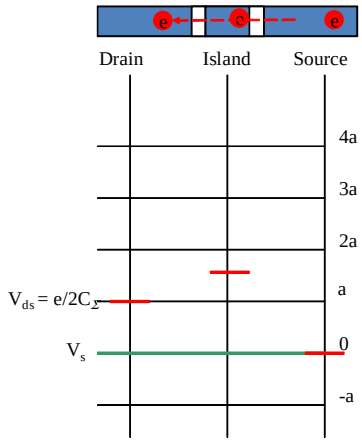


Figure 2.11: Current flow path establishment for Fig. 2.8.

2.2 SET fabrication

A few researchers have reported SET fabrication technology related work [17, 20–36]. There are various patents available which shows detailed SET fabrication methodology [20–22]. The SET based modeling and analysis on fabricated SET is shown in [23]. The demonstration of a SET device fabrication on a single ultra-small silicon quantum dot connected to a gold break junction with a nano-meter scale separation is shown in [24]. The SET fabrication using scaling of nano-wire width from 20 nm down to sub-7 nm regime is shown in [25]. In [17, 26], it is stated that the good etching of the trench between the gate and island in SET leads to good gate isolation and hence, low gate leakage currents. A SET embedded in a nano-mechanical resonator is shown in [27]. Fabrication of Si nano-wires (SiNWs) based SET for room-temperature operation using conventional optical lithography is reported in [28]. The SET fabrication based on germanium quantum-dot and Niobium (Nb) are shown in [29] and [30] respectively. The SET fabrication by current-controlled local oxidation of a two-dimensional electron system and atomic force microscopy (AFM) machining are shown in [31] and [32] respectively. The SET fabrication over silicon-on-insulator (SOI) is shown in [33, 34]. The nanodamascene process for SET fabrication and its co-integration with high-k/metal gate MOSFETs and operation at room temperature (at V_{ds}=0.9 V) with the state-of-the-art nano-wire enabling is presented in [35, 36].

The above research work on SET fabrication shows that it is realizable and practically implementable technology and can be explored further to make effective circuits and systems using SET technology. The fine tuning of capacitances is possible for metallic Ti SETs fabricated on a SiO_2 substrate by the nanodamascene process [36]. This process enables precise positional alignment of the SET metal island to control gate and tunnel junctions. This helps in achieving the capacitances in the range of sub atto-farad which provides room-temperature operation of the device [36, 37]. The present work uses metallic SET parameters from research work carried out in [9, 38] which is based on nanodamascene SET fabrication process. Considering SET as a viable fabrication technology, several researchers have done extensive modeling to simulate SET based circuits.

2.3 SET modeling and characterization

The SET based design is carried out using extensive modeling. Mainly three different approaches have been reported for SET modeling: Monte-Carlo modeling, macro modeling and master equation (analytical) modeling [10, 39]. These modeling approaches are discussed below as:

I In Monte-Carlo modeling, random tunnel times are computed for all possible events and correlation. The core engine of this method is the random number generator. It is based on the fact that the tunneling of electrons is through the tunnel barrier and determined by stochastic process. It is extremely time consuming for large-circuit simulations. Some of the Monte-Carlo simulators are SIMON [40], MOSES [41], KOSEC [42], and SENECA [43]. The Si quantum dot based SET model using Monte Carlo method is shown in [44].

II The other widely used approach is macro modeling. In this approach, SET is replaced by its equivalent circuit that comprises of combination of diodes, resistors, different sources, etc. These can be efficiently implemented in SPICE simulator environments. Kirchhoff's current and voltage laws are incorporated to solve the current-voltage equations. The basis of this method is purely empirical and may not be scalable. The SET macro model is proposed in [45]. The modified SET macro model is described in [46, 47]. The digital inverter implementation for hybrid SET-CMOS using macro modeling is shown in [48].

III In the master equation (analytical) model approach, a set of equations are solved to obtain the characteristics curves of SET. The electron tunnels from source-island-drain, and subsequently the circuit occupies different states. Each of the state differs by external voltages and the charge distribution of the circuit. However, the optimum way to solve the master equation is by considering only a finite number of states. SETTRANS [49] is an example of master equation based SET circuit simulator. The SET model for design and analysis is proposed in [50] and [51]. Additionally, the gate voltage dependency and influence of resistance are incorporated in [52]. The effect

of operating temperature under suitable biasing conditions is analysed in MATLAB [53]. The resistance and the quantum capacitance for CNT based SET are modeled and analysed in [54]. The CB effect of SET is analysed in [55]. The research in [56] shows that the fullerene SET based on QD arrays can overcome the temperature limitation of SET and it can operate at room temperature. The electrical characteristic of SET with aluminium island using neural network is shown in [57].

Monte-Carlo model supports remarkable accuracy of calculation and flexibility of structure configuration. However, this is associated with high computations, large calculation time and compatibility issues with respect to popular SPICE simulator. So, it is suitable for research on SET structure and simulation of small scale SET circuits only. On the other hand, macro model supports fast calculation and outstanding compatibility with present circuit simulators. It is suitable for qualitative analysis of large scale SET and hybrid SET–MOS circuits, but it is limited by relatively smaller accuracy and flexibility. Master equation (analytical) model supports excellent compatibility, high flexibility and accuracy, but the calculation speed is limited for complex designs. This model is suitable for circuit simulation from small to large scale with the balanced configuration of flexibility and speed. From the above, it is envisaged that optimum SET modeling can be achieved by combination of master equation modeling and macro modeling where, the empirical formula of macro model are useful to simplify the master equations. For SET based complex circuit designs, there is a need of physical parameter based, accurate and compact analytical model that support design and development using CAD tools. Mahapatra *et al.* have proposed a Mahapatra–Ionescu–Banerjee (MIB) model for SET-based circuit design [10, 58]. During the verification, Mahapatra et al. have verified the model accuracy with Monte Carlo (MC) simulation tool SIMON [10]. They have reported the accuracy results with respect to various characteristics curves. It has been observed that the MIB model results are in good correlation with respect to SIMON tool. It provides flexibility to modify SET parameters as there is no fixed, unified technology for SET fabrication. Same authors have provided Verilog-A model for efficient usage with CAD [59]. In the

proposed work, SET based computing system is designed using MIB dual gate SET model with zero background charge on the island.

The important relations between the electrical and physical parameters that must be satisfied for its implementation are as follows:

– The electrostatic charging energy $E_c = e^2/2C_\Sigma$

– The operating temperature $T \propto e^2/2k_B C_\Sigma$.

– The voltage level $V \propto e^2/2k_B C_\Sigma$

– The device maximum operating frequency $\propto 1/R_t C_\Sigma$,

– The SET inverting voltage gain is $\propto 1/A_V = C_g/C_j$

Here, e is electron charge, C_Σ is total capacitance on the island and k_B is Boltzmann's constant. For a robust reliable design of SET logic, which can operate with the least possible error at room temperature, the charging energy E_c must be as large as possible compared with the thermal energy. For the present design $e^2/C_\Sigma = 40k_B T$ is considered by selecting SET physical parameters *i.e.* capacitance between different terminals. From eq. 2.5 and eq. 2.8, the proposed SET works at voltage and temperature values of more than 520 mV and 300 K respectively.

The biasing of two gate terminals enables switching ON/OFF of the SET device for different configuration like, PSET and NSET [60]. It also explores basic SET based block level designs using these configurations. Fig. 2.12 illustrates the symbolic representation of SET for Cadence Virtuoso schematic editor including SET parameters. The SET parameters considered for the proposed research work are C_s = C_d = 0.03 aF, C_g = 0.045 aF, C_b = 0.05 aF, R_s = R_d = 1 MΩ. The SET parameters are opted from research work carried out in [9, 38] for room temperature operation and operating voltage of 0.8 V. Also, these SET parameters are within the fabrication range for room-temperature operation [36]. The research work in [9] verifies the simulation characteristics of SET with the fabricated I–V characteristics.

The model setup for SET current–voltage characterization measurements is shown in Fig. 2.12. In the figure, V_{ds}, V_{gs} and V_{bs} symbols represent drain to source voltage, control gate to source voltage and tuning gate to source voltage respectively. Fig. 2.13(a) shows I_{ds}–V_{ds} characteristics where V_{gs} is varied from 0 V to 1.6 V in the step of 0.4 V and V_{bs} is applied to 0 V. The width of the

Coulomb gap reduces from a maximum to zero. Fig. 2.13(b) shows the I_{ds}–V_{gs} characteristics where V_{ds} is varied from 0 V to 1.6 V in step of 0.4 V and V_{bs} is applied to 0 V. This I–V characteristics are well defined by Coulomb oscillations measurements [17, 61]. It can be seen that the current increases in magnitude as V_{ds} increases. The oscillating nature of SET is due to tunneling effect and Coulomb blockade phenomena. The current oscillates with the period e/C_g. The oscillating nature of SET helps in multi-valued and multi-gate design implementation. Using a literal gate (SET, MOSFET and constant current source) ADC, multi-valued adder and multi-valued SRAM can be designed [9]. In the proposed work, the oscillating nature is useful to achieve N-type SET (NSET) and P-type SET (PSET) characteristics. Fig. 2.13(c) shows the I_{ds}–V_{gs} characteristics where, V_{ds} is 0.8 V and V_{bs} is applied to two different voltages of 0 V and 0.8 V. It shows that V_{bs} of 0.8 V gives nearly 90° phase shift to I_{ds} of Fig. 2.13(b). The present work considers $V_{ds} = V_{gs} = V_{bs} = 0.8$ V. The expanded range of V_{gs} for 0 V to 0.8 V from Fig. 2.13(c) is shown in Fig. 2.13(d). It clearly identifies effect of V_{bs} on I_{ds}–V_{gs} that helps to achieve characteristics as similar to existing PMOS and NMOS transistors. The connection to tuning gate (g2) of SET to ground ($V_{bs} = 0$ V) enables SET to act in PSET configuration whereas connection to supply voltage ($V_{bs} = 0.8$ V) makes SET works as NSET configuration. This characteristic of SET facilitates to design the SET based logic gates. Also, the MATLAB modeling for the PSET and NSET configurations are shown in Section 5.1. The designs carried out with SET are discussed in next section.

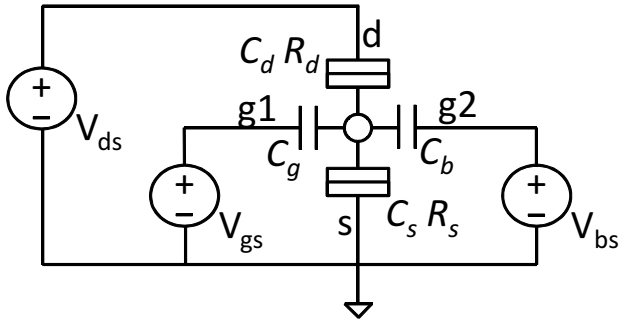


Figure 2.12: Model setup for SET current–voltage characterization measurements. Drain, Source, control gate and tuning gates are connected with V_{ds}, ground, V_{gs} and V_{bs} respectively.

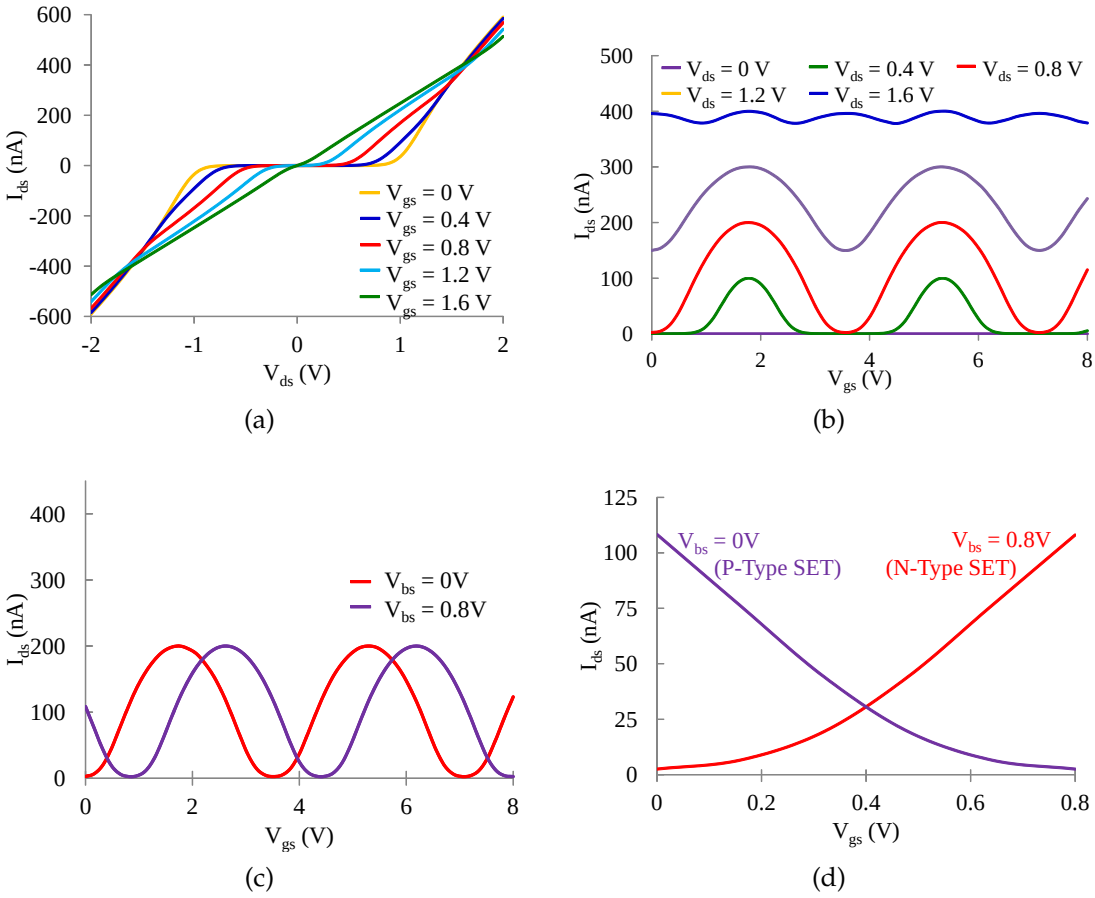


Figure 2.13: SET I–V characteristics measurements. (a) I_{ds}–V_{ds} characteristics, V_{gs} varies from 0 V to 1.6 V in 0.4 V steps and V_{bs} is 0 V. (b) I_{ds}–V_{gs} characteristics, V_{ds} varies from 0 V to 1.6 V in 0.4 V steps and V_{bs} is 0 V. (b) I_{ds}–V_{gs} characteristics, V_{ds} is 0.8 V, V_{bs} is 0 V and 0.8 V. (d) Expanded I_{ds}–V_{gs} characteristics of Fig. 2.13(c) for V_{gs} of 0 V to 0.8 V.

2.4 SET based designs

The fabrication and modeling of SET enables various SET based designs in analog and digital domains. The viability of SET technology with existing MOSFET technology is already explained in previous sections. It is investigated that the current driving capacity and power dissipation of SET and CMOS technology are complementary to each other [9]. To alleviate this issue, co-integration of SET with CMOS has been proposed as one of the prospective solutions. This can also convey new functionalities. The hybrid SET-MOSFET based designs are discussed in Section 2.4.1. The SET is a promising and prominent nano device because of its ability to dissipate power in ultra-low range. Hence, only SET based design is

a prospective solution and can efficiently replace conventional MOS technology. This has been explored and vividly discussed in Section 2.4.2.

2.4.1 Hybrid SET-MOSFET based designs

The research performed in [62, 63] present the SET-MOSFET based hybrid designs by behavioral modeling. The impact of energy quantization in SET with CMOS integrated circuits is discussed in [64]. The compatibility and realization of SET-CMOS hybrid integrated logic operation at 22 nm is explored in [11, 38, 65, 66]. Hence, the SET based computing system can be heterogeneously integrated with CMOS designs. Using this concept different digital logic block designs such as inverter [67–69], transmission gate [70], basic logic circuits [71, 72], reversible logic gates [73], programmable logic array (PLA) [74], encoder/decoder [75], octal to binary encoder [76], odd parity generator and parity checker [77], logic error detector [78], summation circuit [79], binary-coded decimal (BCD) adder [80], 4-bit parallel adder/subtractor [81], 4-bit ALU [82], reversible logic based ALU [83], multiplier [84], digital-to-analog converter (DAC) [85, 86], analog-to-digital converter (ADC) [86–88], voltage controlled ring oscillator [89], frequency multiplier [90] and hybrid memory cell [91–93], have been implemented.

Research work in [94] shows hybrid MOS and SET architectures towards arithmetic applications. The SET's quantum dot location and FET device dimension variations are analysed in [95]. The first SET with high-k/metal gate operating at room temperature (at V_{ds}=0.9V) co-integrated with fully depleted SOI MOSFET (with 20 nm gate length) to realize a hybrid SET-FET circuit is shown in [96]. Experimental demonstration of hybrid CMOS-SET and the effect of SET tunneling resistance variations on hybrid circuit design are carried out in [97] and [98] respectively. The CMOS electronics for the readout of SET at very low temperature is shown in [99]. From the above reviewed papers, it is investigated that several researches have been performed in the field of designing circuits using hybrid SET-MOSFET technology. However, modern algorithms, memories, processors, etc. demand high density and high performance while maintaining low power consumption. Relatively hybrid SET-MOSFET technology requires large number

of MOS transistors and concurrently power dissipation increases for complex hybrid designs. The low-power operation of IC requires reduction in both the total capacitance of circuits and operation voltage. These are difficult to attain with present MOS technology. SET is a promising and prominent nano device because of its ability to dissipate power in ultra-low range. Hence, only SET based design is a prospective solution and can efficiently replace conventional MOS technology. This has been explored and vividly discussed in the next subsection.

2.4.2 Only SET based designs

In this section the designs carried out with only SET technology are discussed. The research related to single electron devices is shown in [17, 61]. Tucker proposed the replacement of FET with SET in complementary-type logic gates have much smaller size [100]. In [10, 18] it is discussed that SET can be used to define the single bit of information by the presence/absence of electrons at conducting islands. This leads to minimal static and leakage current loss in SET based device. Using SET technology basic gates [101–105], periodic symmetric functions generation [106], ultra-high frequency operation [107], half adder [108], 4 x 1 multiplexer [109, 110], D-type flip flop [111, 112], 3-bit multiplier [113], frequency doubler [114], random number generator [115], 4-bit ADC [116], and 8 x 8 Memory [117] have been designed.

The different research work (last five years) related to hybrid SET-MOS and only SET technologies are also detailed and effectively tabulated in Table 2.2. It addresses block level logic circuits comprising with one or more constraints related to design and simulation. Hybrid SET-MOSFET circuits have been initially explored to achieve low power and better performance to complement SET drawback of low driving capability. But, the design parameters for hybrid circuits are restricted for operation at either lower temperature or lower voltage or with unrealistic SET parameters.

Table 2.2: Comparison of SET based work carried out in last 5 years

Ref.	Year	Technology	Design	Temp.	Number of Transistors / Junctions	I/O (V)	Freq.	Delay	Power	Simulator	Research gap / Remark
[66]	2020	Hybrid	Buffer	300 K	4	0.8/0.8	100 MHz	577.5 ns	96.59 nW	Spectre	-
[86]	2020	Hybrid	ADC	144 K	12	0.1/-	1 GHz	-	29.2 nW	PSPICE	-
[73]	2020	Hybrid	Fredkin gate	77 K	13	0.8/0.8	-	-	1.08 uW	SPICE	-
[117]	2019	Only SET	8 x 8 Memory	300 K	-	0.8/0.8	4 GHz	4 ps	830 nW	Spectre	Without Interconnect parasitics
[110]	2019	Only SET	Data transfer system	-	-	0.016/ 0.016	-	9.8 ns	239.2 pW	SIMON	-
[70]	2019	Hybrid	T Gate	300K	16	0.8/0.8	-	2 ns	2.05 uW	SPICE	-
[75]	2019	Hybrid	NOR2 (Encoder)	300 K	20	0.7/0.7	-	42 ps	2.05 uW	SPICE	-
[107]	2018	Only SET	Ultra high-frequency characteristics	1.55 K	-	-	1 THz	-	-	SIMON	Without Interconnect parasitics and Unrealistic SET parameters
[114]	2018	Only SET	Frequency Doubler	15-300 K	2	0.25/ 0.18	1 GHz	-	-	HSPICE	
[116]	2018	Only SET	4-bit ADC	100 K, 300 K	8	-/0.012	-	-	-	SIMON	
[62]	2018	Hybrid	Inverter	30 K	2	0.195/-	-	-	-	SPICE	-

Ref.	Year	Technology	Design	Temp.	Number of Transistors / Junctions	I/O (V)	Freq.	Delay	Power	Simulator	Research gap / Remark
[112]	2017	Only SET	Flip Flop	-	8	0.1/0.1	-	-	-	SIMON	-
[65]	2017	Hybrid	4X1 multiplexer	300 K	46	0.8/0.8	-	-	2.6 nW	TCAD	-
[78]	2017	Hybrid	Error detection	-	-	2.4/-	-	-	-	SPICE	-
[106]	2016	Only SET	Periodic symmetric functions	300 K	2	-/0.016	-	-	-	SIMON	Without Interconnect parasitics and Unrealistic SET parameters
[79]	2016	Hybrid	Half adder	-	-	0.8/0.8	-	-	2.6 uW	-	-
[74]	2016	Hybrid	PLA	-	48	0.3/0.3	-	3.2 ns	144 nW	SIMON	-

The limitations of a SET are background charge, fabrication, lower temperature operation, low drive current, etc. With the advancement of technology and several state-of-the-art researches in this area, these limitations can be largely mitigated. The background charge can be overcome by a variable capacitor usage [118]. It changes the transfer function of SET. The latest nanodamascene fabrication process enables room temperature operation [35, 36] with enhanced SET driving capability [11]. The low drive current can be improved by implementing parallel SET devices [11]. The SET to MOS drive capabilities are explored in [9, 65, 66]. The hybrid SET-MOS circuits have the fabrication challenge as it needs both the transistors with different fabrication process on the same IC. In the case of only SET based designs, they are not working at room temperature and CMOS compatible voltages. Also, these designs have a fewer number of transistors and usage of basic SPICE level simulator tools. The latest nanodamascene fabrication process enables room temperature operation with enhanced SET driving capability motivated to design of promising applications like, logic and high density memory (Table 2.2, [115]). This design is carried out by our group and uses same specifications as in the proposed design. The research in [11] shows design, analytical derivations and simulation regarding SET driving capability for high fan out requirements of hybrid SET-MOS and only SET based circuits. The previous work of different SET domains directs road-map for complex logic circuits using SET technology in near future.

2.5 SET based computing system

Various aspects of SET technology are presented in previous sections. It is investigated that till date the maximum research work in SET based design domain is up to block level designs only. High-end computing system is vital to today's business needs. These are the fast and most powerful machines with hundreds of thousands of processors. It consists of multistage (pipeline) functional units, CPUs, multiple cores, fast central registers, large and fast memory, and fast communication units. Presently Intel processors like core i7, core i5 uses

tri-gate (3D) transistor that has increased surface area of each transistor on the chip while reducing leakage power which consequently decreases significant power consumption. To achieve better performance than existing systems, a new information processing technology must be explored. It should be compatible with a system architecture that can fully utilize the new device. Perhaps at that stage answer may be SET, an emerging technology based on quantum mechanics that makes use of electron tunneling and CB. SET is a nano size transistor that offers low power consumption and high operating speed, room temperature operation and retains its performance even on an atomic scale. Besides this, it can control the motion of a single electron. The goal is to use SET as building blocks to match the design requirements when compared its counterparts. To meet these requirements, a SET based computing system is designed and verified that can be integrated on top of a CMOS carrier to achieve added functionality without utilizing important silicon space. At the present stage, the proposed design may not serve all the aforesaid features of high-end computing system. But, the design demonstrates the feature of multiple instruction executions at CMOS compatible voltage and room temperature. With current status of SET research, it can be foreseen that such a development is not far from reality. Future, computing system systems are likely to have extreme power constraints, leading to clock rates similar to today's systems, extreme scalability and performance irregularity. SET based computing system will have power and performance advantage. The detailed design of a SET based computing system is discussed in next chapter.

CHAPTER 3

SET Based Computing System Design

This chapter describes the design of SET based computing system. The Section 3.1 briefly describes generalized computing system, overview of design methodology and proposed SET based computing system design parameters. The Section 3.2 covers execution aspect of proposed design. Sections 3.3–3.8 of this chapter describe the designs of SET based circuit blocks and computing system. The computing system is designed with bottom-up approach where individual blocks are designed and verified for timing and parametric analyses. The timing analysis results are presented with corresponding circuit design whereas the parametric analysis results are discussed in Chapter **??**.

3.1 Brief discussion of the proposed work

3.1.1 Description of the computing system

In order to select the computing system for design, various factors are considered like design architecture, implacability, verification, enhancement, etc. The implanted design is based von-Neumann architecture which is adopted from [14]. In the proposed design, it is enhanced for 14 different instructions with in-housed 16x8 memory. The block diagram of 8-bit computing system is presented in Fig. 3.1. The computing system consists of a program counter (PC), a memory access register (MAR), a 16x8 memory (with an address decoder), an instruction register (IR), an instruction decoder (ID), a controller, an ALU, a register-A (accumulator), a register-B and tri-state buffers [14]. The PC tracks the record of program execution.

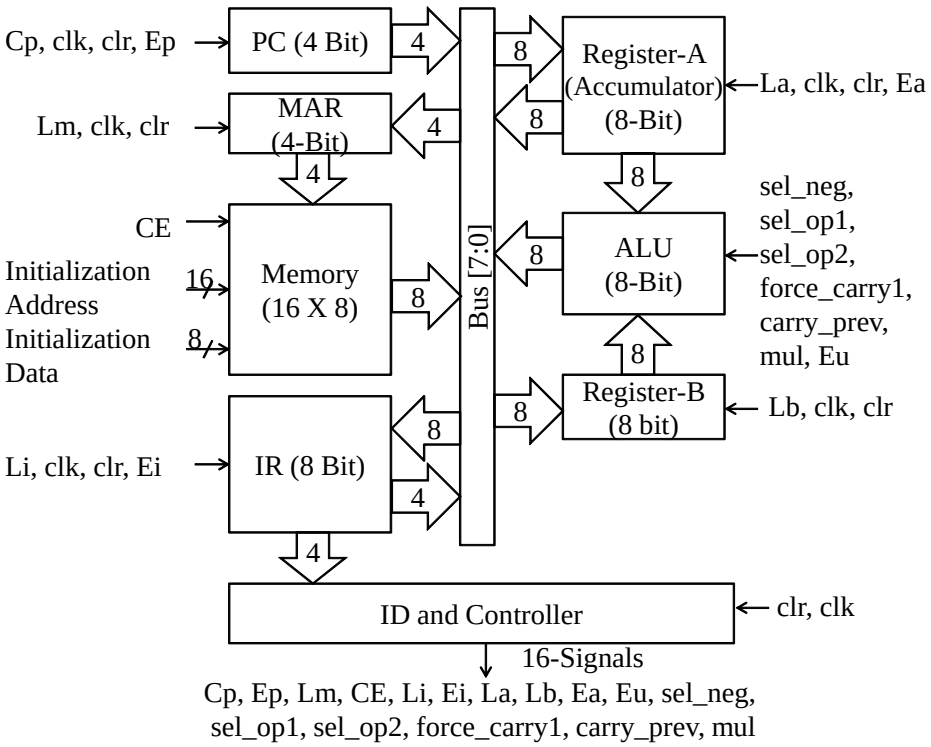


Figure 3.1: The block diagram of computing system showing circuit blocks and associated signals.

The output of PC is latched to MAR that refers to address location of 16x8 memory. The 16x8 memory stores instructions and data, which is latched to the IR. The controller knows the status of IR information that is either instruction or data. For the case of instruction, the ID and controller process the read-out information according to the instruction. For the case of data, it is latched to register-A or B and desired operation is performed by ALU. The ALU performs arithmetic and logic operation based on the control signals provided by the controller. The tri-state buffers connect the blocks of the computing system by eight signals that is referred as 'Bus [7:0]' in Fig. 3.1. The controller enables these tri-state buffers on 8-bit bus to control the data flow and avoid data contention which is discussed in Section 3.7.

The computing system instruction set architecture (ISA) supports execution of 14 instructions as described in Table 3.1. The 8-bit instruction comprises of two nibbles. The four most significant bits (MSB) refers to the upper nibble while remaining four least significant bits (LSB) denotes the lower nibble. The upper nibble is defined as opcode, whereas the lower nibble is the address pointer of the data (operand) stored in 16x8 memory. The instruction format with its execution

flow chart is shown in Fig. 3.2. Each of the instruction execution takes place in 6 clock cycles. The first 3 cycles (instruction fetch) are common for each of the instruction. It performs PC read and latch to MAR, PC increment and instruction read from memory operations. The remaining 3 cycles are instruction opcode specific. It performs memory data (operand) read and process with registers or ALU as per opcode. For 'LDA' and 'LDB' instructions, the controller enables registers and stores memory readout data in it. For 'MOV' instruction, the controller generates control signals to read the data from register-B and writes to register-A. For 'OUT' instruction, the controller latch register-A data to the tri-state buffer as the output result. For 'NOP' instruction, the controller makes no change to system registers and ALU. For other arithmetic and logical instructions ('ADD', 'SUB', 'ANA', 'ORA', 'XRA', 'CMA', 'RLC', 'RRC'and 'MUL') the controller generates control signals for ALU to process on the data.

Table 3.1: Description of supported instructions by SET based computing system

Mnemonics	**Opcode**	**Description (X and Y are 4-bit data)**
LDA, XY	0	Load Accumulator from content of memory location Y
LDB, XY	1	Load Register-B from content of memory location Y
MOV, XY	2	Move content from Register-B to Accumulator
ADD, XY	3	Add XY to Accumulator
SUB, XY	4	Subtract XY from Accumulator
ANA, XY	5	Logical AND of XY to Accumulator
ORA, XY	6	Logical OR of XY to Accumulator
XRA, XY	7	Logical XOR of XY to Accumulator
CMA, XY	8	Complement content of Accumulator
RLC, XY	9	Shift Left the content of Accumulator with appending 0 to LSB
RRC, XY	A	Shift Right the content of Accumulator with appending 0 to MSB
MUL, XY	B	Multiply content of Accumulator lower nibble with Y
OUT, XY	C	Outputs contents of Accumulator to data bus
NOP, XY	D	No change in computing system state

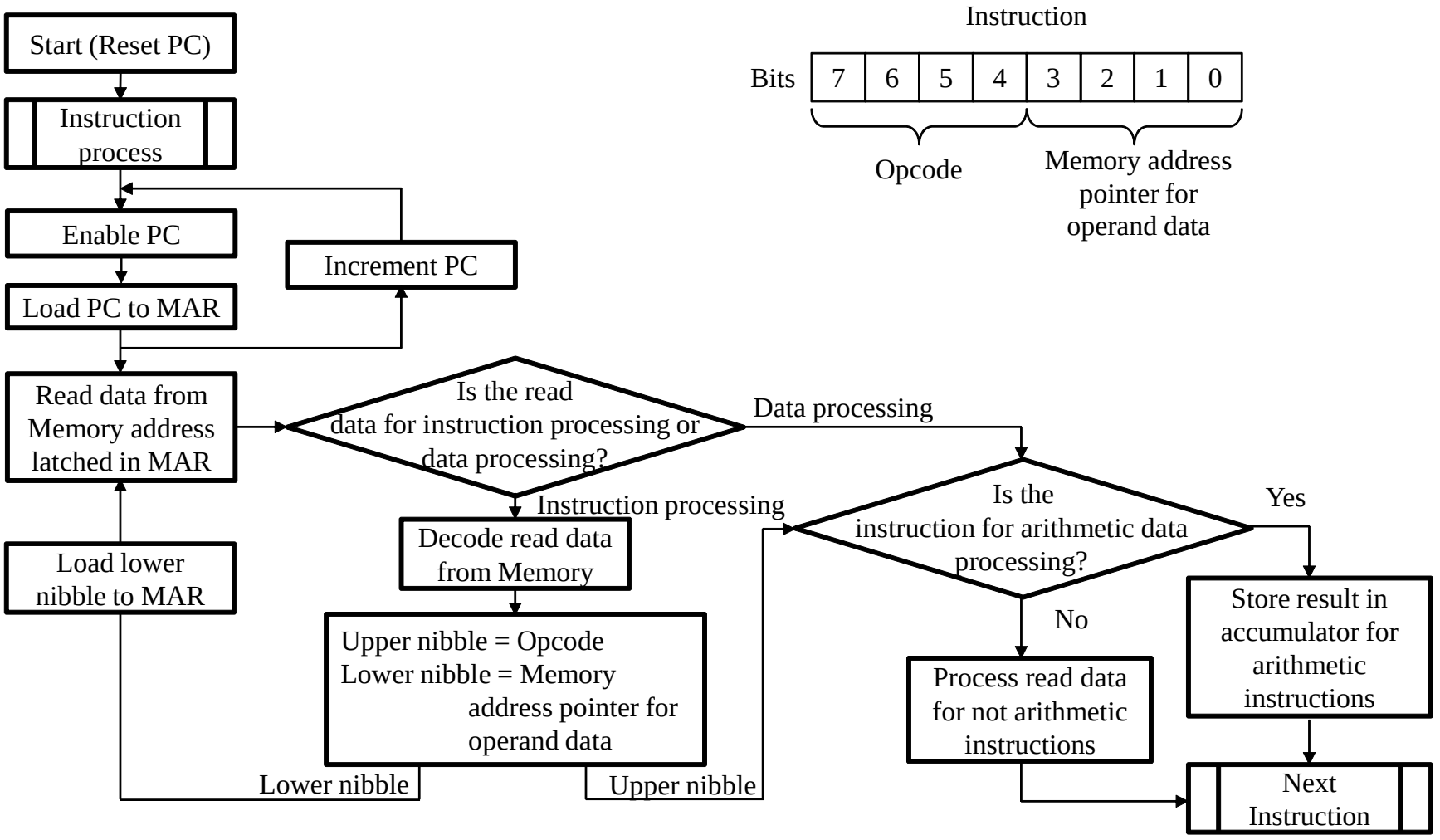


Figure 3.2: The flow-chart for instruction execution.

3.1.2 SET based computing system design methodology

The proposed research work carries out the SET based computing system design. The complex systems are often designed using very high speed integrated circuit hardware description language (VHDL) or Verilog. The design can be carried out at algorithm level, register transfer level (RTL) level or gate level. Major designs are carried out at RTL level as it is synthesizable. The synthesizer converts RTL design to gate level design for selected fabrication technology library. But, for SET technology such synthesizer is not available and design needs to be carried out with transistor level abstraction.

Fig. 3.3 shows the different levels of abstractions for design. The current research work is carried out in two abstract levels structural (red arrow path) and behavioral (blue arrow path). The structural design is carried out in using Cadence Virtuoso whereas behavioral scheme is used for program level simulation.

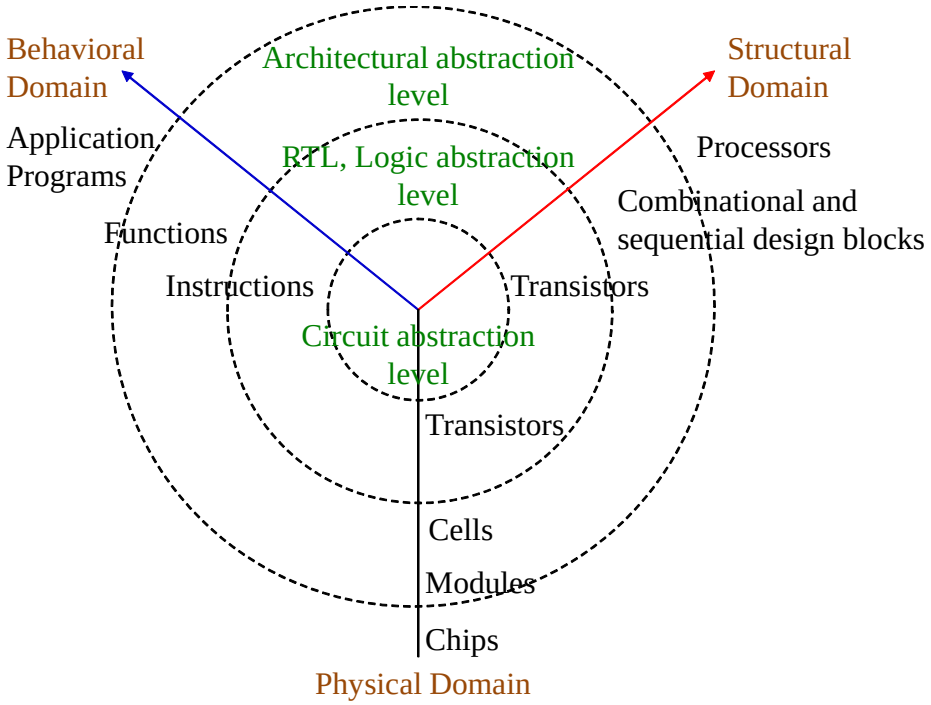


Figure 3.3: Design abstraction levels.

3.1.3 Discussion on SET and interconnect parameters

The metallic SET transistors can be fabricated within the chip interconnect layers which can be stacked above the CMOS platform by the BEOL fabrication process[38]. The proposed work considers SET parameters which are based on nanodamascene fabrication process for room-temperature operation [36]. The opted SET parameters are $C_s = C_d = 0.03$ aF, $C_g = 0.045$ aF, $C_b = 0.05$ aF, $R_s = R_d = 1$ MΩ for room temperature operation and operating voltage of 0.8 V from [9]. The simulation characteristics of SET with the fabricated I–V characteristics are detailed in [9, 38]. The SET based interconnect capacitance is computed based on the SET fabrication parameters for the BEOL fabrication process [119]. The interconnect parasitic capacitance calculation refers to Ti nanowire parameters of 15 nm width, 5 nm height and 45 nm thickness of SiO_2 layer on Si wafer [38, 120]. Considering 38 nm pitch [121] and parallel plate method, the capacitance measures to 0.224 aF. Every design node of SET based computing system incorporates this capacitance during simulation and verification.

3.2 Execution of SET based computing system design

The execution of SET based computing system design requires different tools and softwares for its implementation, verification and analysis. For emerging nano-technology like SET, there is no such synthesizer or library available. So, the SET based computing design is carried out at gate level abstraction. The design uses Cadence Virtuoso schematic editor for design entry, Cadence analog design environment (ADE) for simulation through Cadence spectre, Cadence waveform viewer for viewing the signals and Cadence calculator for measurements [122]. The Microsoft Visual Basic is used for design and development of vector file generation tool development.

Fig. 3.4 shows the SET based computing system design steps along with the associated tool with colored text in the legend. It shows that the design is carried out by modifying SET parameters in Verilog-A model file of SET. The model is imported in Cadence Virtuoso and a dual gate SET symbol is generated. The SET

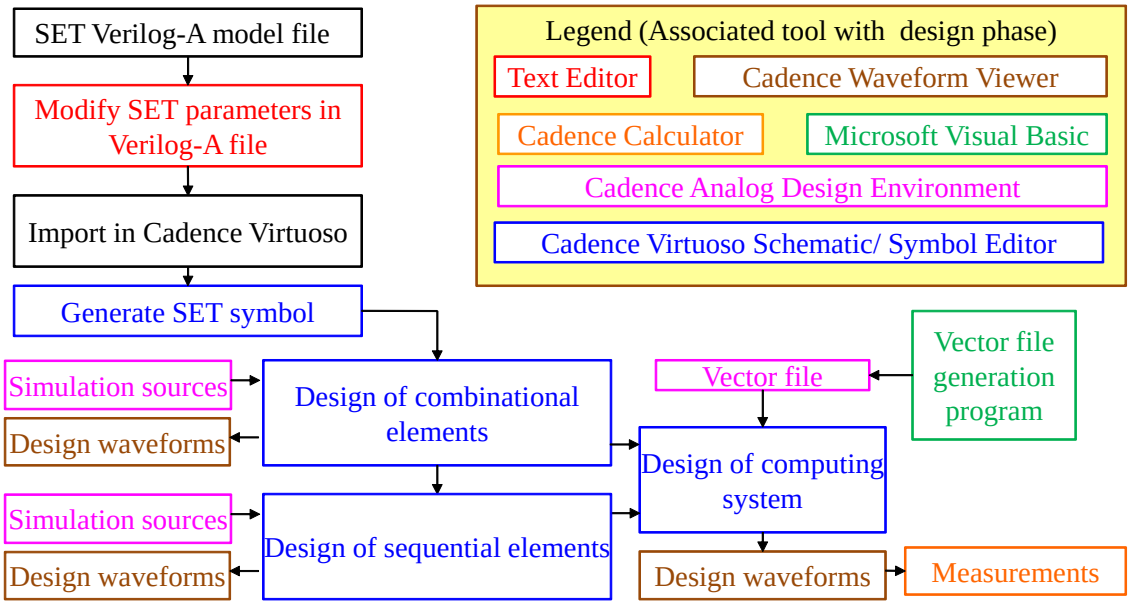


Figure 3.4: SET based design flow for computing system design with associated tool.

symbol is a basic building block for designing the combinational and sequential elements. The verification of each of the design block is carried out by providing stimuli to inputs and monitoring outputs on waveform viewer. The detailed design and verification of the computing system is described in subsequent sections.

The hierarchical design of SET based computing system with bottom-up approach is shown in Fig. 3.5. The figure also describes reference section of design circuit block. These foundation blocks can be correlated to computing system elements as shown in Fig. 3.1. The brief description of subsequent sections are as follows:

– Section 3.3 details about designing of combination elements for the SET based computing system. It includes design of SET based 2-inputs NAND gate, 2-inputs NOR gate, 2-inputs XOR gate, tri-state buffer, 2x1 multiplexer and full adder. These designs are realized using PSET and NSET with similar design methodology as CMOS logic.

– Section 3.4 describes SET based ALU design. The ALU performs arithmetic and logic operations for 'ADD', 'SUB', 'ANA', 'ORA', 'XRA', 'CMA', 'RLC', 'RRC' and 'MUL' instructions. The controller of the computing system provides control signals to ALU for each of the instruction execution.

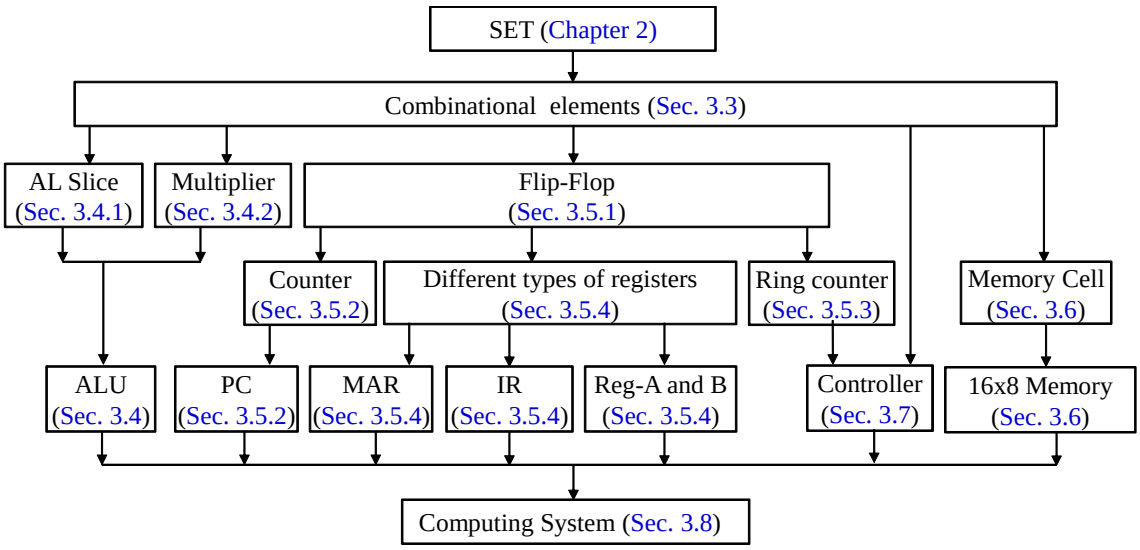


Figure 3.5: Hierarchy of SET based computing system design.

– Section 3.5 presents details of SET based sequential elements. The design of D-Flip flop, 4-bit binary counter, 6-stage ring counter and 4-bit register are described in this section. The 4-bit counter is used as PC in the computing system. The ring counter is used in controller design. The 4-bit registers are used for latch and store intermittent data on the computing system bus. The computing system has seven 4-bit registers namely; a MAR, two each for IR, data A and data B.

– Section 3.6 details SRAM design. The SRAM is used for storage of computer instruction and associated data. The SRAM has 16 locations of memory which stores 8-bit data.

– Section 3.7 presents controller design. The controller manages instruction and data flow in the computing system by generating signals for all circuit blocks of the computing system. These signals are generated with falling edge of clock and used by relevant circuit blocks with the rising edge of the clock to avoid meta-stability.

– Section 3.8 shows the design of computing system using integration of essential circuit blocks.

3.3 Design of SET based elementary combinational circuits

In this section, the designs of SET based combinational logic blocks are described. It includes design of SET based basic gates (inverter, 2-inputs NAND gate, 2-inputs NOR gate, 2-inputs XOR gate and tri-state buffer), 2x1 multiplexer, 2x4 decoder and full adder.

3.3.1 Design of a SET based basic gates

The circuit diagram of a SET based inverter is shown in Fig. 3.6(a). The test bench model for SET based inverter is illustrated in Fig. 3.6(b). The test circuit has symbolic representation of SET based inverter. The inverter is simulated for DC analysis and transient analysis. Fig. 3.6(c) shows the DC transfer characteristics of the SET based inverter circuit. For DC analysis measurements the control gate of each SET (g1) is connected to input voltage V_{in} which is a voltage sweep from 0 to 0.8 V. The DC analysis of SET based inverter circuit shows maximum and minimum output voltages as 786.5 mV and 10.4 mV respectively. This analysis is helpful in determining effective full scale output of SET based circuit. The transition threshold of SET based inverter is at 400 mV. The transient analysis of SET based inverter is shown in Fig. 3.6(d). For transient analysis, the input to inverter is connected by pulse source. The pulse source has amplitude of 0.8 V and rise and fall duration of 1 ps. Subsequent SET based designs use similar test bench model for design verification and thus it is not shown in respective section.

The circuit diagram of a SET based 2-inputs NAND gate is shown in Fig. 3.7(a). The signals 'A' and 'B' are inputs to NAND gate which are connected to pulse sources in test bench model. The 'out' is the output of NAND gate. The transient analysis of 2-input NAND gate is shown in Fig. 3.7(b). Using the same methodology multiple inputs NAND gates are designed and simulated. By adding an inverter at the NAND gate output, AND gate functionality is achieved.

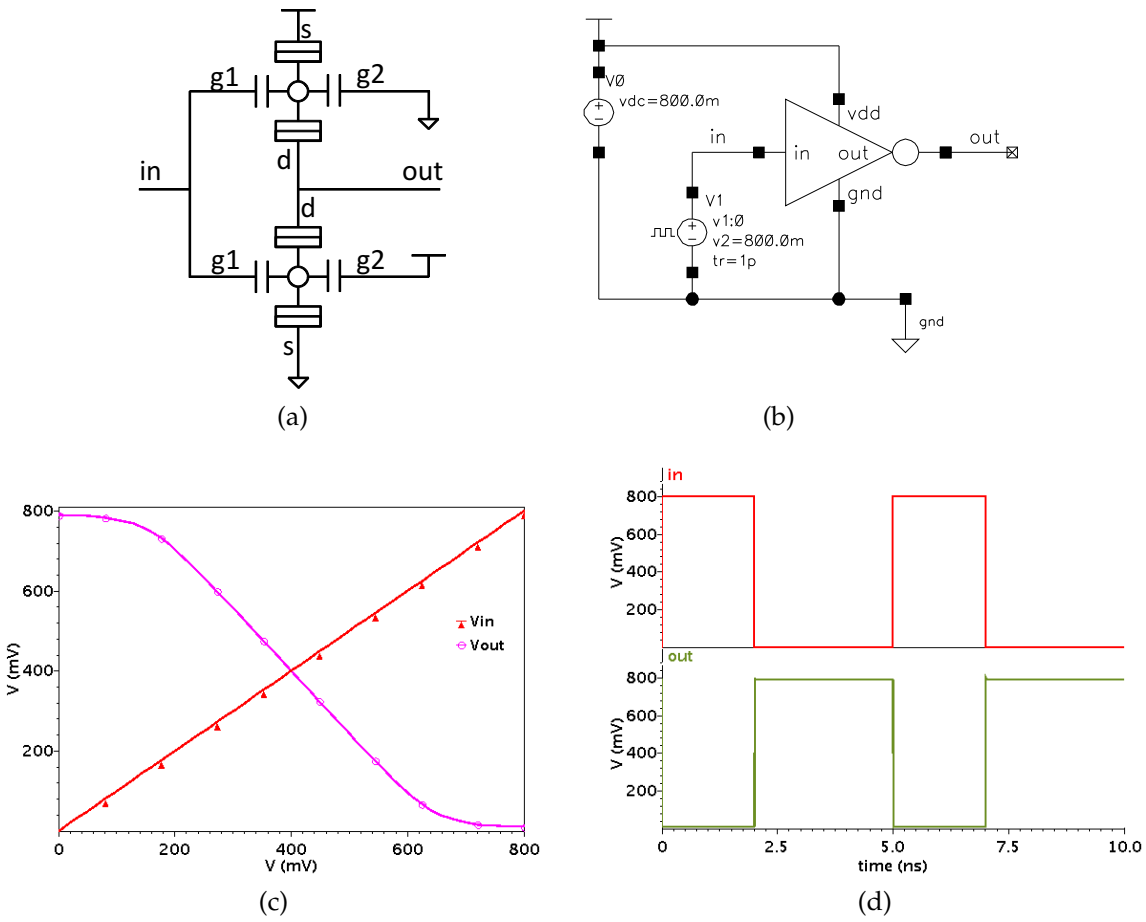


Figure 3.6: Design of SET based inverter. (a) Circuit diagram. (b) Test bench model. (c) DC characteristics. (d) Transient analysis.

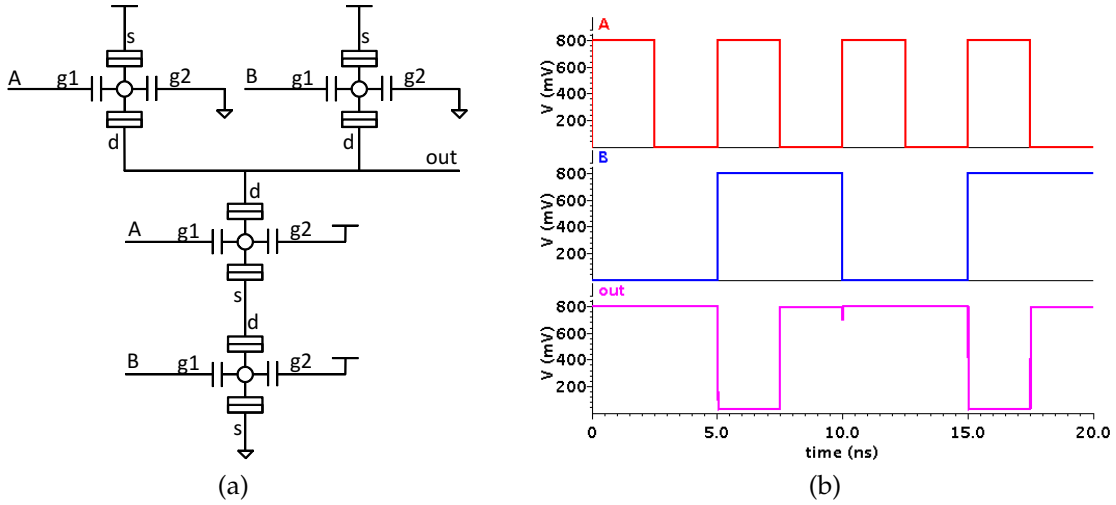
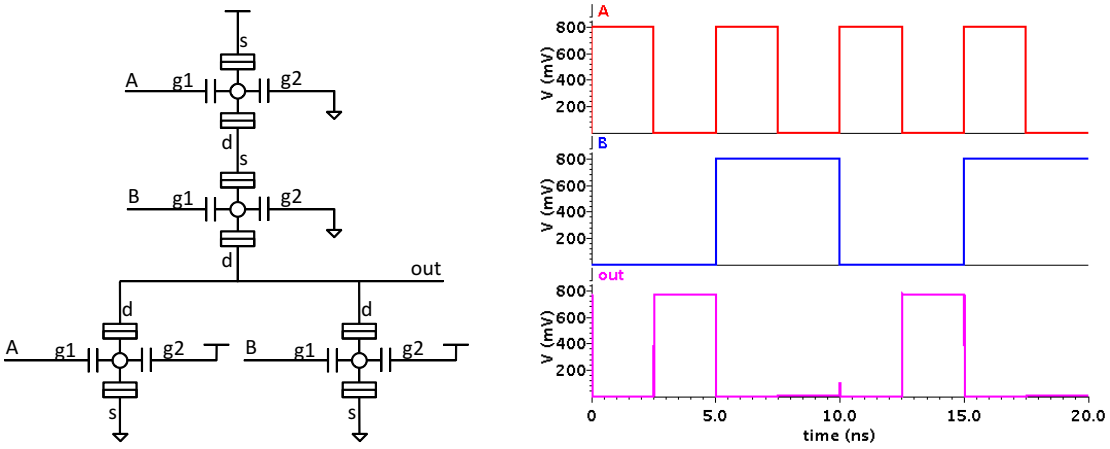


Figure 3.7: Design of SET based 2-inputs NAND gate. (a) Circuit diagram. (b) Transient analysis.

The circuit diagram of a SET based 2-inputs NOR gate is shown in Fig. 3.8(a). The signals 'A' and 'B' are inputs to NOR gate which are connected to pulse sources in test bench model. The 'out' is output of NOR gate. The transient analysis of 2-input NOR gate is shown in Fig. 3.8(b). Using the same methodology multiple inputs NOR gates are designed and simulated. By adding an inverter at the NOR gate output, OR gate functionality is achieved.

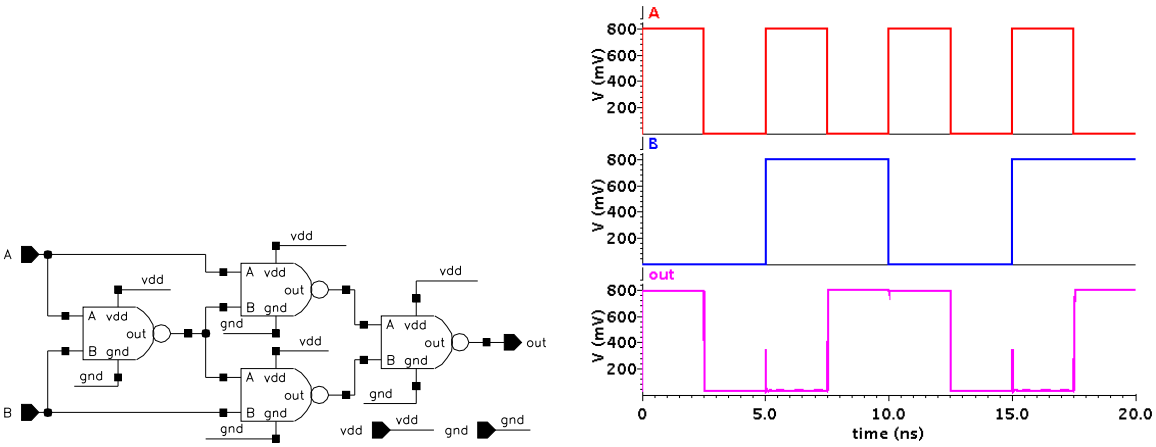


(a) (b)

Figure 3.8: Design of SET based 2-inputs NOR gate. (a) Circuit diagram. (b) Transient analysis.

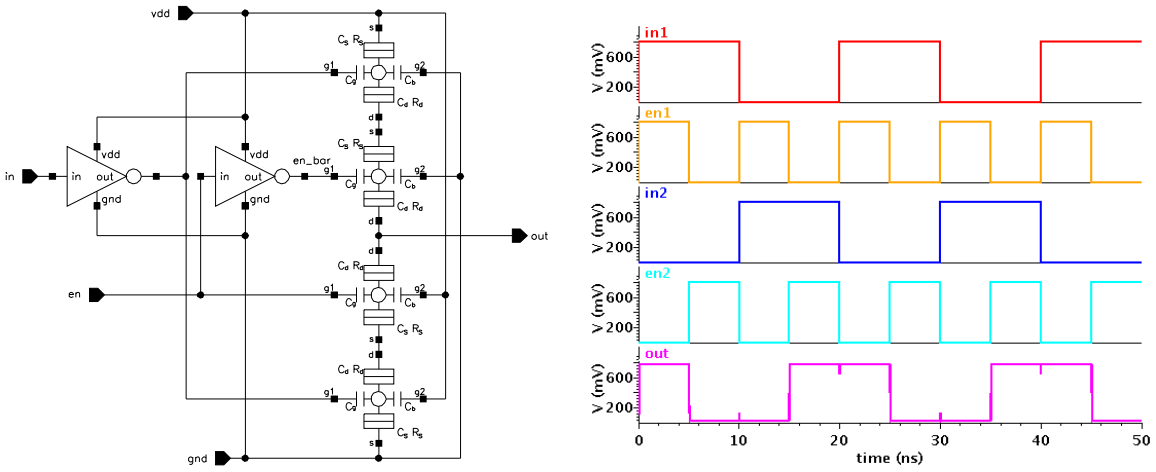
The circuit diagram of a SET based 2-inputs XOR gate design is shown in Fig. 3.9(a). The signals 'A' and 'B' are inputs to XOR gate which are connected to pulse sources in test bench model. The 'out' is output of XOR gate. The transient analysis of 2-input XOR gate is shown in Fig. 3.9(b).

The circuit diagram of a SET based tri-state buffer is shown in Fig. 3.10(a). It is difficult to verify the individual tri-state buffer as when 'en' is low, the output is floating. So, the verification of design is carried out by shorting the outputs of two tri-state buffers. This simulates actual design condition where multiple outputs are shorted on 'Bus [7:0]' as shown in Fig. 3.1. The signal 'in1' and 'en1' are inputs to tri-state buffer-1. The signal 'in2' and 'en2' are inputs to tri-state buffer-2. The transient analysis of tri-state buffers is shown in Fig. 3.10(b). It shows that the 'out' follows input 'in1' when 'en1' is high and follows input 'in2' when 'en2' is high. The output 'out' is indeterminate stage when 'en1' and 'en2' are low.



(a) (b)

Figure 3.9: Design of SET based 2-inputs XOR gate. (a) Circuit diagram. (b) Transient analysis.



(a) (b)

Figure 3.10: Design of SET based tri-state buffer. (a) Circuit diagram. (b) Transient analysis.

3.3.2 Design of a SET based 2x1 multiplexer

The circuit diagram of a SET based 2x1 multiplexer is shown in Fig. 3.11(a). The signals 'A', 'B' and 'sel' are inputs to 2x1 multiplexer which are connected to pulse sources in test bench model. The 'out' is output of 2x1 multiplexer. The transient analysis of 2x1 multiplexer is shown in Fig. 3.11(b). The figure shows that 'sel' selects either input 'A' or 'B' and directs to 'out' based on its polarity of low or high respectively.

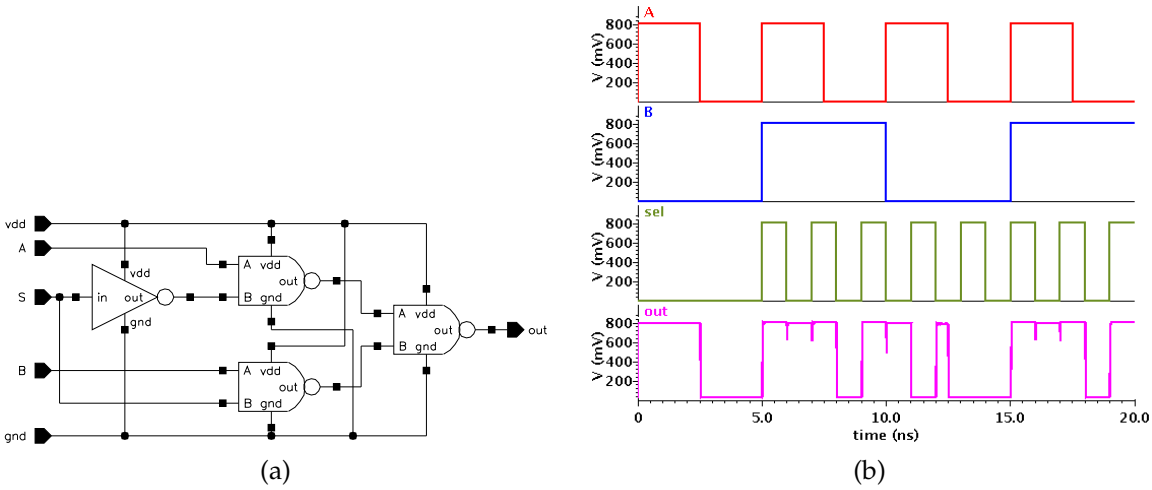


Figure 3.11: Design of SET based 2x1 multiplexer. (a) Circuit diagram. (b) Transient analysis.

3.3.3 Design of a SET based 2x4 decoder

The circuit diagram of a SET based 2x4 decoder is shown in Fig. 3.12(a). The signals 'A0', 'A1' and 'En' are inputs to 2x4 decoder which are connected to pulse sources in test bench model. The 'D[3:0]' are outputs of 2x1 decoder. The transient analysis of 2x4 decoder is shown in Fig. 3.12(b). Using the similar design a SET based 4x16 decoder design is carried out.

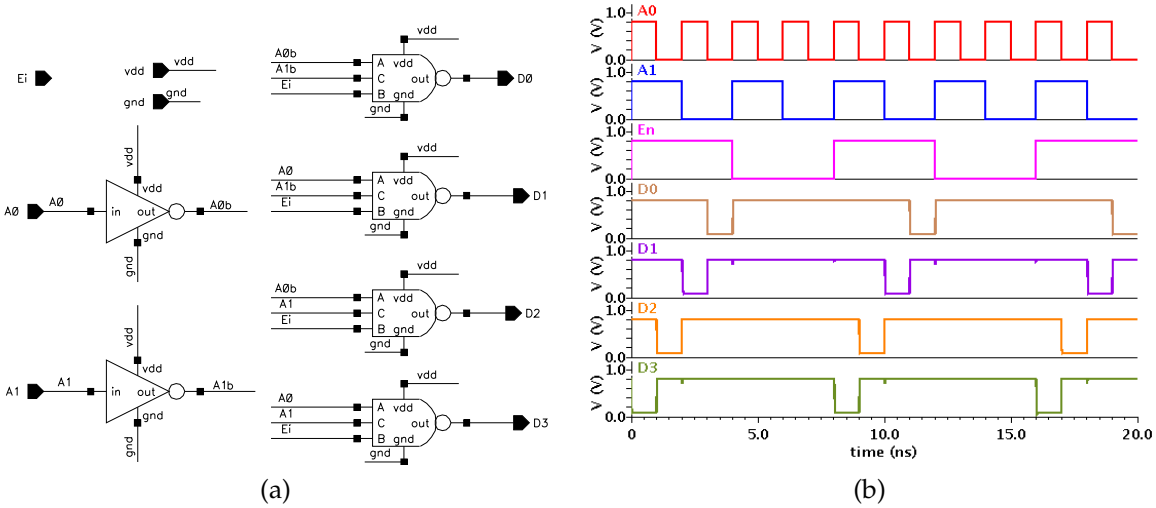
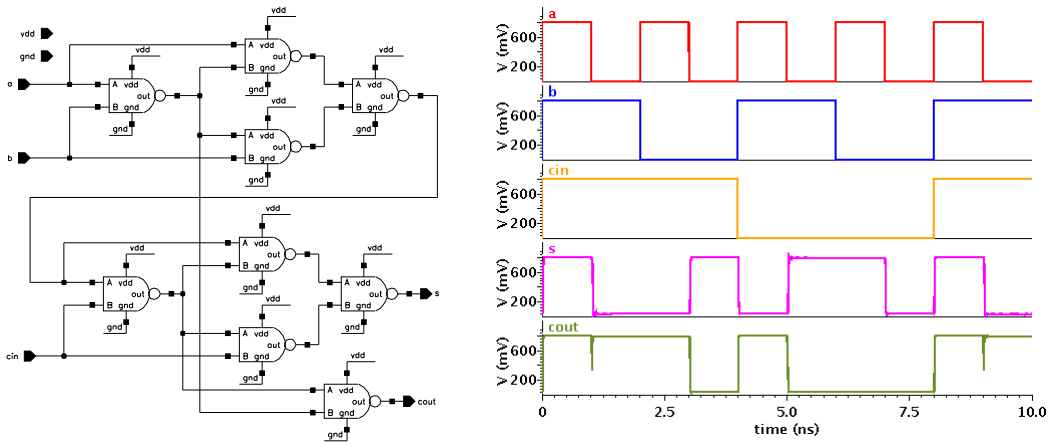


Figure 3.12: Design of SET based 2x4 decoder. (a) Circuit diagram. (b) Transient analysis.

3.3.4 Design of a SET based full adder

The circuit diagram of a SET based full adder design is shown in Fig. 3.13(a). The signals 'a', 'b' and 'cin' are inputs to full adder which are connected to pulse sources in test bench model. The 's' and 'cout' are outputs of full adder. The transient analysis of full adder is shown in Fig. 3.13(b).



(a) (b)

Figure 3.13: Design of SET based full adder. (a) Circuit diagram. (b) Transient analysis.

3.4 Design of SET based ALU

The ALU performs arithmetic and logic operations for 'ADD', 'SUB', 'ANA', 'ORA', 'XRA', 'CMA', 'RLC', 'RRC' and 'MUL' instructions. The block diagram of SET based ALU design is shown in Fig. 3.14. The ALU receives two 8-bit data inputs from computing system registers. These data is processed as per the signals generated by controller for each instruction. The ALU comprises of three basic components as: 1) eight cascaded arithmetic-logic (AL) slices, 2) a 4-bit multiplier and, 3) a 16x8 multiplexer. The SET based ALU design is carried out by slice architecture so that it can be further extended using cascade inputs [123]. The AL slice of ALU is a circuit block that performs desired function on two operands of one bit each. The cascading of eight AL slices results in 8-bit functionality. The AL slice performs the arithmetic (except multiplier) and logic functions. The multiplication

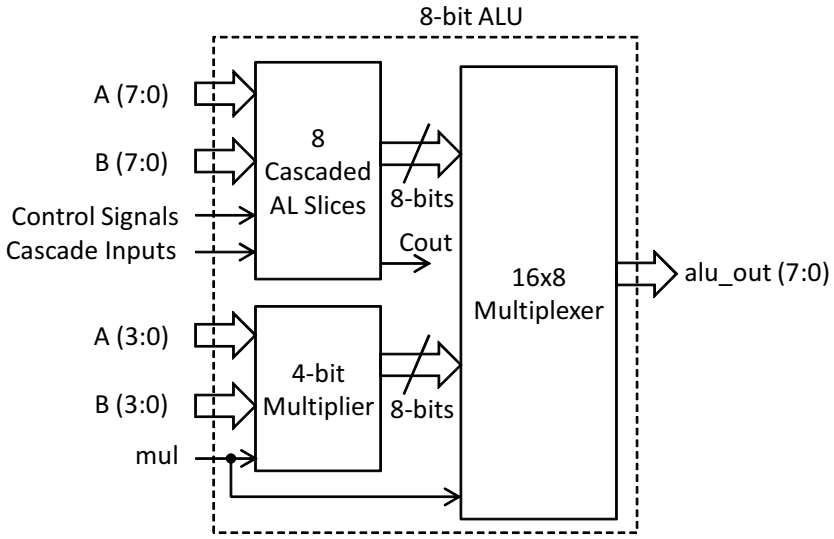


Figure 3.14: The block diagram of SET based 8-bit ALU.

operation can be accomplished using AL slices by repetitive addition operation. Henceforth, to fasten up the ALU processing, a dedicated multiplier block is incorporated that performs multiplication of two 4-bit numbers and generates 8-bit output. The 16x8 multiplexer selects the output of either 8-bit of AL slices or a 4-bit multiplier depending on 'mul' control signal. The 16x8 multiplexer consists of eight 2x1 multiplexers as discussed in Section 3.3.2.

3.4.1 Design of a SET based AL slice

The circuit diagram of a SET based AL slice is shown in Fig. 3.15. The AL slice is designed with SET based inverter, NAND gate, NOR gate, AND gate, OR gate and combination of these gates. The hardware design of the AL slice shows that it performs operation on two input signals, 'A' and 'B'. The AL slice performs desired operation based on the six input control signals; namely 'sel_neg', 'sel_op1', 'sel_op2', 'shift_r', 'force_carry1' and 'mul_r'. Table 3.2 describes each control signal value for specified instruction. Based on the values of input, control and cascade signals, the AL slice generates 'carry' and 'result' outputs. Each AL slice comprises of 74 SETs. The associated vector file for AL slice design verification is listed in Appendix A.1. The transient analysis of AL slice is shown in Fig. 3.16. The transient analysis shows results for addition, subtraction, logical AND, logical OR, logical XOR, rotate right and complement functions during time interval of 0-8

Table 3.2: Details of SET based ALU control signals

ALU	Instruction								
Control Signals	**ADD**	**SUB**	**ANA**	**ORA**	**XRA**	**CMA**	**RLC**	**RRC**	**MUL**
sel_neg	0	1	0	0	0	0	0	0	0
sel_op1	1	1	1	0	1	1	1	0	0
sel_op2	0	0	1	0	0	0	0	1	1
shift_r	0	0	0	0	0	0	0	1	0
force_carry1	0	0	1	1	1	1	0	1	0
mul	0	0	0	0	0	0	0	0	1
carry_prev	1	0	0	1	1	1	1	0	0

ns, 8-16 ns, 16-20 ns, 20-24 ns, 24-28 ns, 28-36 ns, 36-40 ns respectively. The input pattern of verification is selected such that it covers all operation of AL slice with possible input conditions.

Fig. 3.17 shows the schematic of eight AL cascaded slices that fulfills the requirements of 8-bit data processing system. Each slice has one bit input data from 'A(7:0)' and 'B(7:0)' respectively. The control signals are commonly connected to each slice. The 'carry_prev' and 'Anext' are cascade inputs that are used to cascade multiple AL slices. The 'carry_prev' is connected to *AL slice 0* for inclusion of external carry. The 'carry' and 'carry_prev' are inverted polarity signals. The 'Anext' is connected to *AL slice 7* to route external input during rotate right operation.

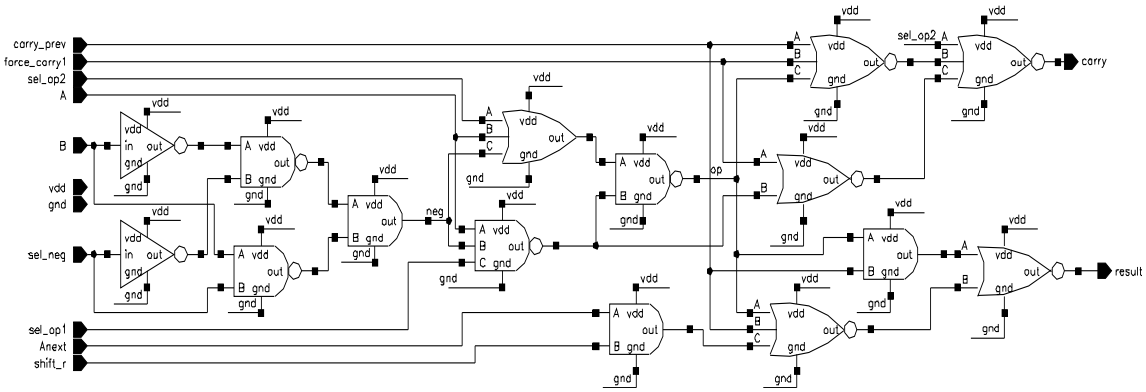


Figure 3.15: Circuit diagram of a SET based AL slice.

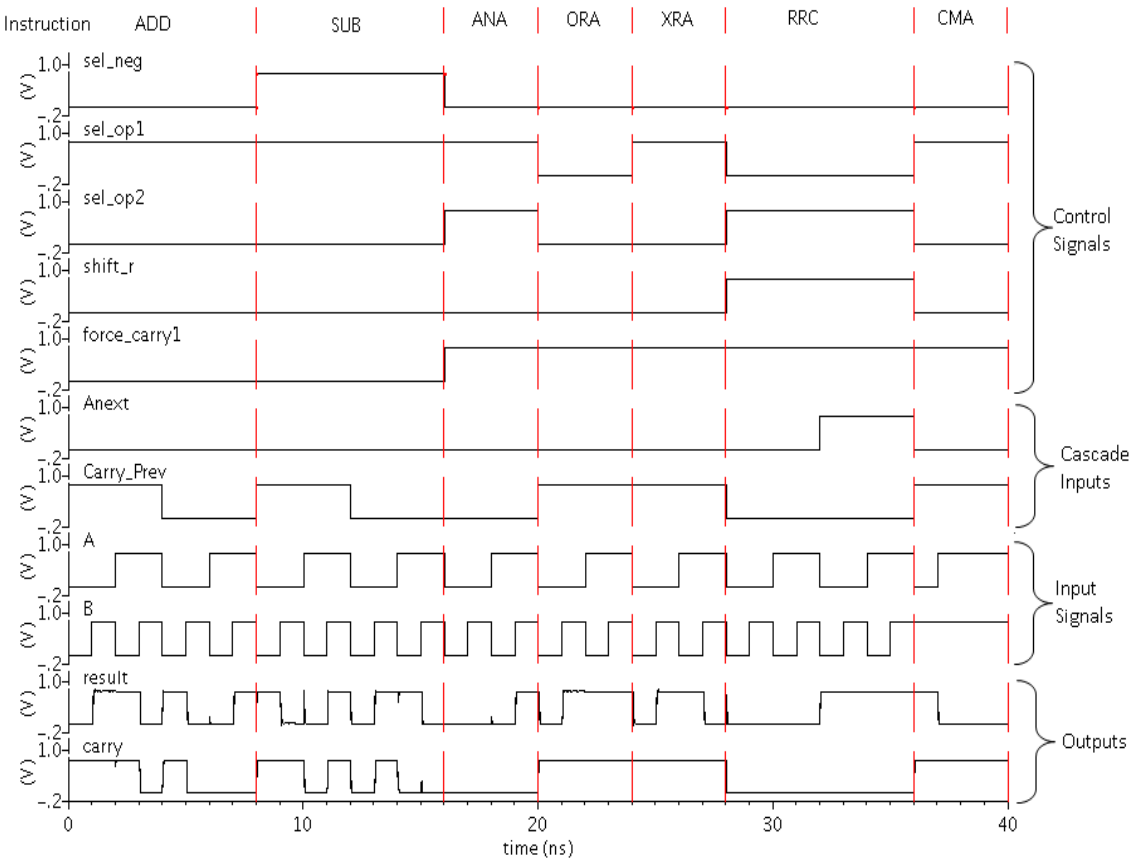


Figure 3.16: Transient analysis of a SET based AL slice.

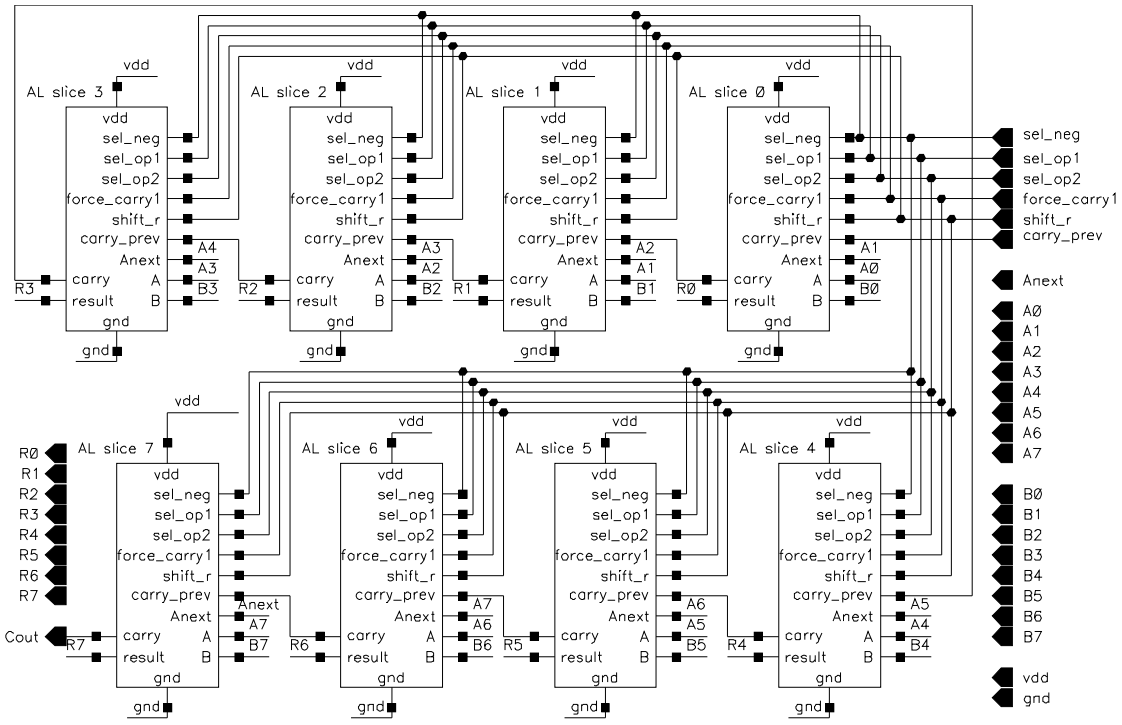


Figure 3.17: Circuit diagram of cascade eight AL slices.

3.4.2 Design of a SET based multiplier

The multiplication operation can be implemented using successive additive operations. However, to achieve faster execution, a separate 4-bit binary multiplier is incorporated in the presented ALU design. It performs multiplication with single 'MUL' instruction. The design of multiplier cell is shown in Fig. 3.18 which consists of an AND gate and a full adder.

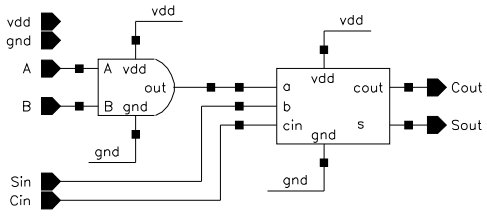


Figure 3.18: The circuit diagram of multiplier cell.

The circuit diagram of a SET based 4-bit multiplier is shown in Fig. 3.19. The 4-bit multiplier consists of 12 *multiplier cells* and 7 AND gates which perform binary multiplication. The 4-bit multiplication generates 8-bit output and requires 558 SETs. The verification of design is carried out using vector file which is listed in Appendix A.2. The Fig. 3.20 shows the transient analysis 4-bit multiplier for square function implementation. The waveforms of Fig. 3.20 are decimal representation of grouped signals which are

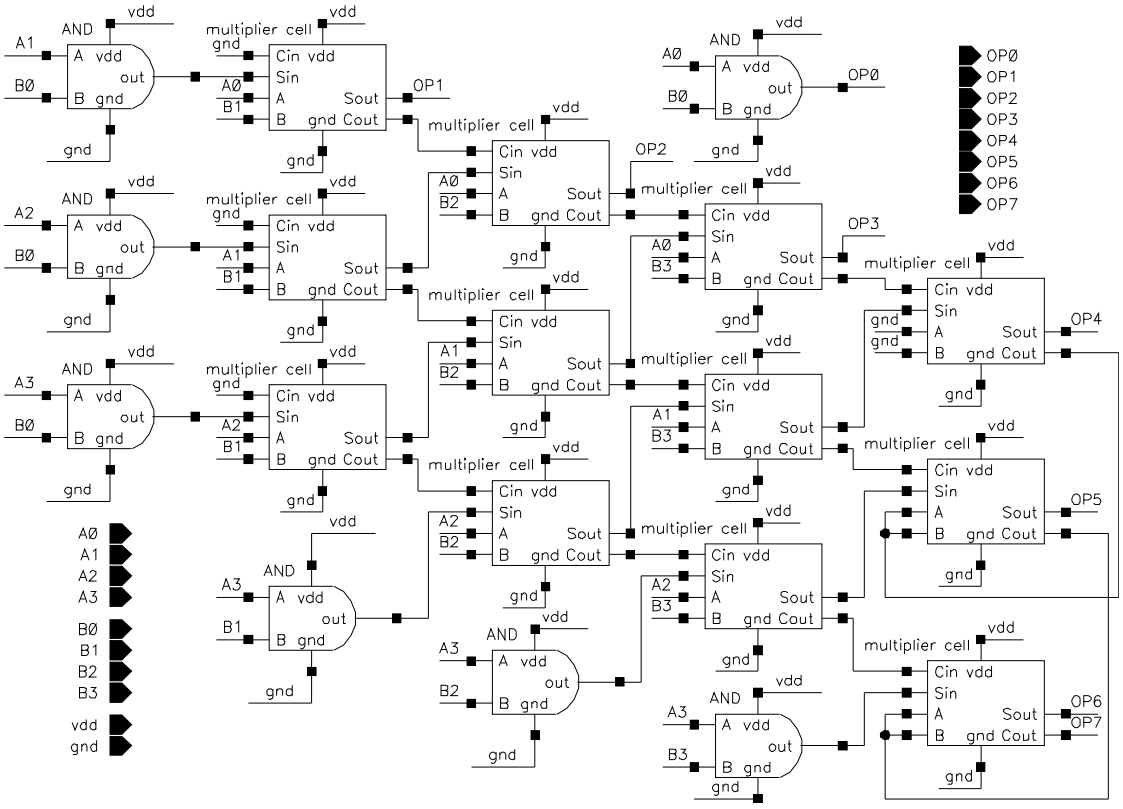


Figure 3.19: Circuit diagram of a SET based 4-bit multiplier.

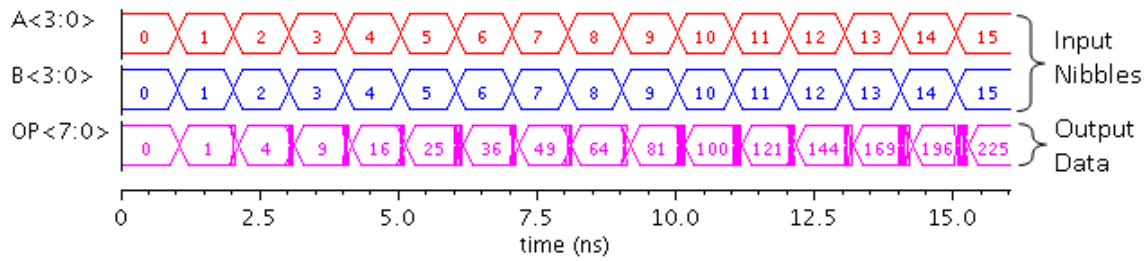


Figure 3.20: Transient analysis of a SET based 4-bit multiplier.

converted from analog to digital at 0.4 V threshold. The 8-bit ALU schematic design is shown in Fig. 3.21 that is detailed representation of block diagram shown in Fig. 3.14.

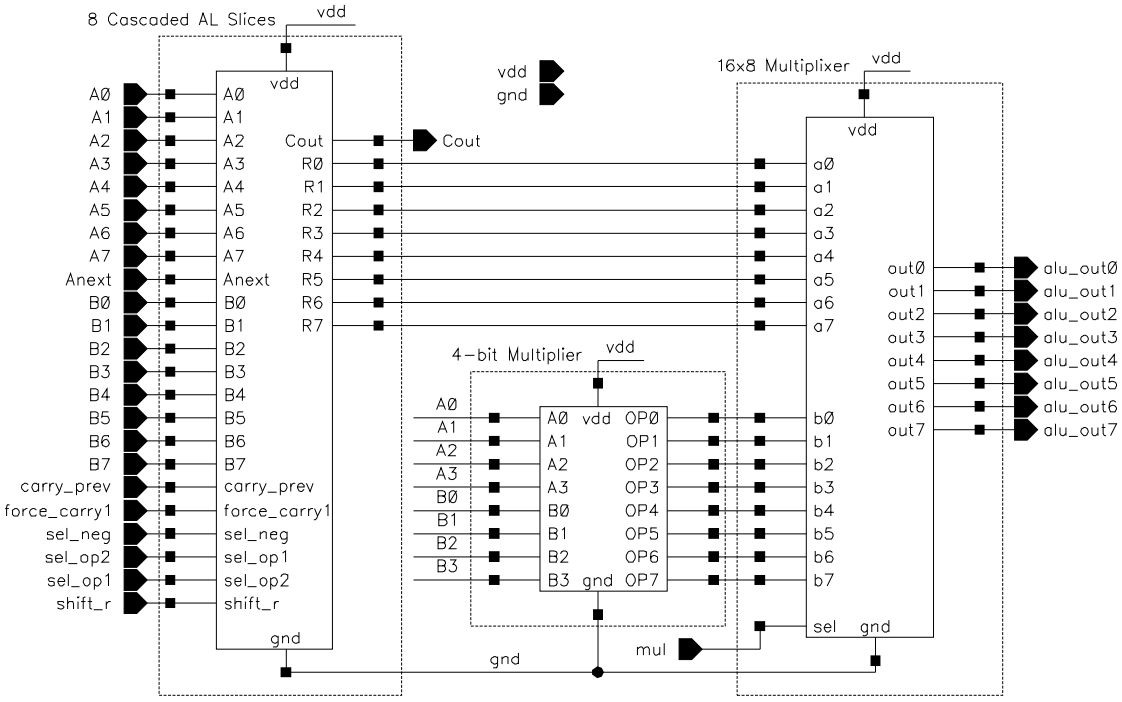


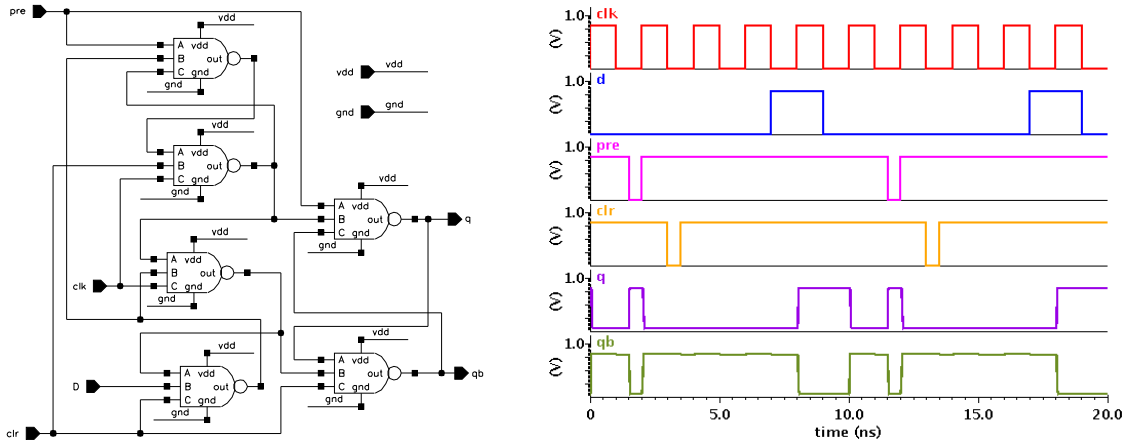
Figure 3.21: Circuit diagram of SET based ALU.

3.5 Design of SET based elementary sequential circuit blocks

In this section, various designs of SET based sequential logic blocks are described. It includes design of SET based D Flip-flop, 4-bit binary counter, 6-stage ring counter and 4-bit register.

3.5.1 Design of a SET based D Flip-flop

The circuit diagram of a SET based D Flip-Flop is shown in Fig. 3.22(a). The transient analysis of D Flip-flop is shown in Fig. 3.22(b). The input signals 'clk', 'd', 'pre' and 'clr' provide inputs as clock, data, preset and clear respectively. The edge triggered D Flip-flop generates 'q' and its complemented output 'qb'. The input data 'd' is transferred with respect to clock 'clk' to the output 'q'. The 'pre' and 'clr' force the output 'q' to logic high (0.8 V) and logic low (0 V) with respect to clock 'clk'.

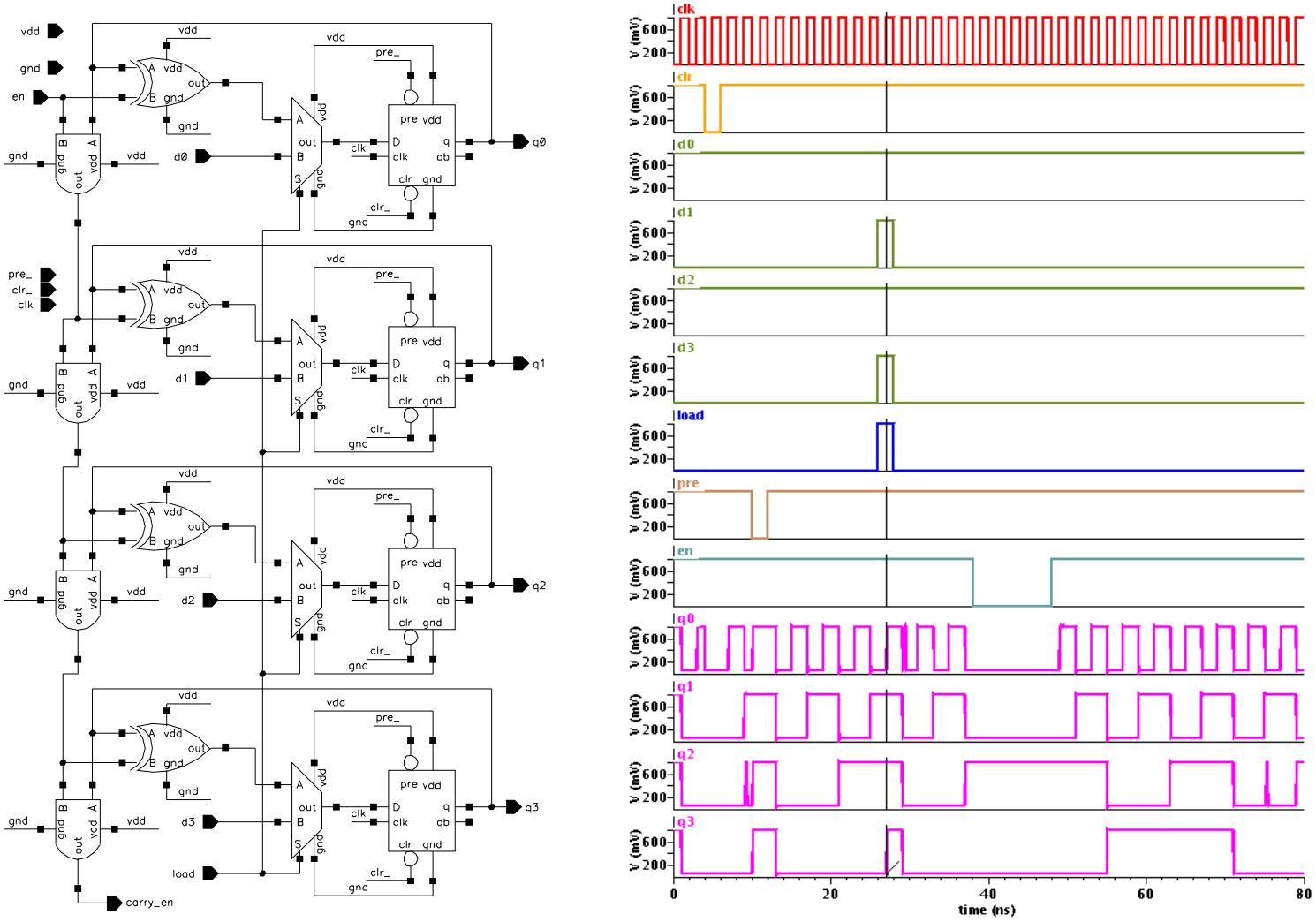


(a) (b)

Figure 3.22: Design of SET based D Flip-flop. (a) Circuit diagram. (b) Transient analysis.

3.5.2 Design of a SET based 4-bit counter

The circuit diagram of a SET based 4-bit counter is shown in Fig. 3.23(a). The verification of design is carried out using a vector file which is listed in Appendix A.3. The transient analysis of 4-bit counter is shown in Fig. 3.23(b). The input signals 'clk', 'd(3:0)', 'load', 'en', 'pre' and 'clr' provide inputs as clock, data, load, enable, preset and clear. The 4-bit counter generates 'q(3:0)' and 'carry_en' outputs. The 'load' loads data 'd(3:0)' with respect to clock 'clk'. The 'pre' and 'clr' force the outputs 'q(3:0)' to logic high "1111" and logic low "0000" with respect to clock 'clk'. The 'en' enables 'q(3:0)' to increment when it is high or output remains in previous value. The 'carry_en' output is used to cascade the counter to higher bits.

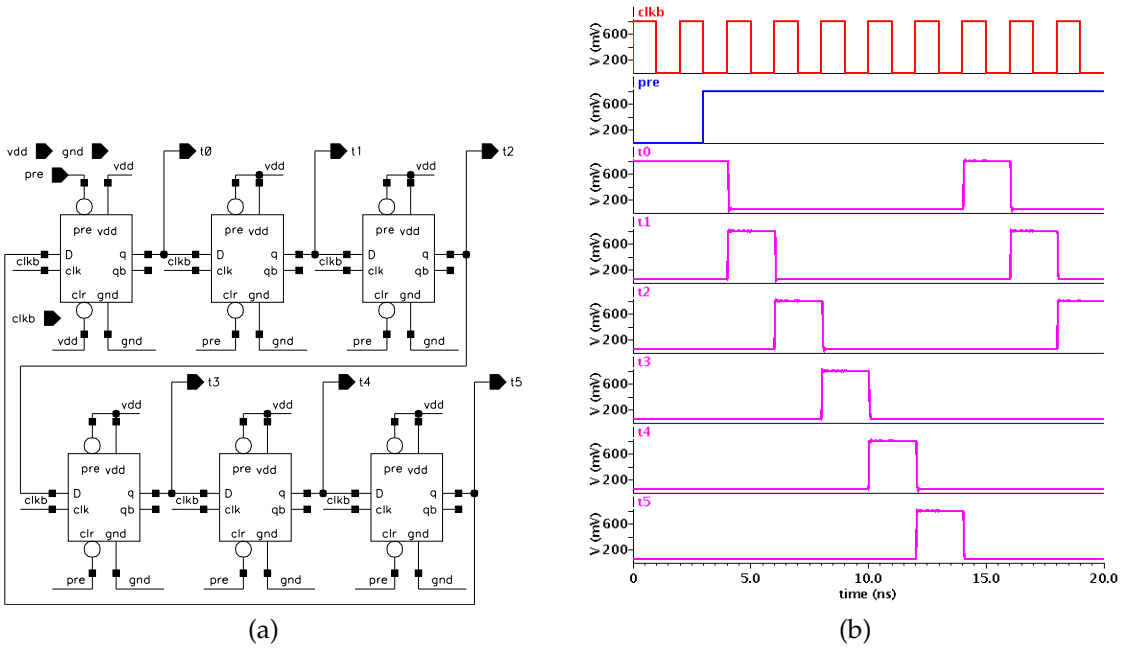


(a) (b)

Figure 3.23: Design of SET based 4-bit counter. (a) Circuit diagram. (b) Transient analysis.

3.5.3 Design of a SET based ring counter

The circuit diagram of a SET based ring counter is shown in Fig. 3.24(a). The transient analysis of ring counter is shown in Fig. 3.24(b). The input signals 'clk' and 'pre' provide inputs as clock and preset respectively. These input signals are generated by different pulse sources. The ring counter generates 't(5:0)' outputs. The 'pre' generates 't0' output high and 't(5:1)' outputs to low states.

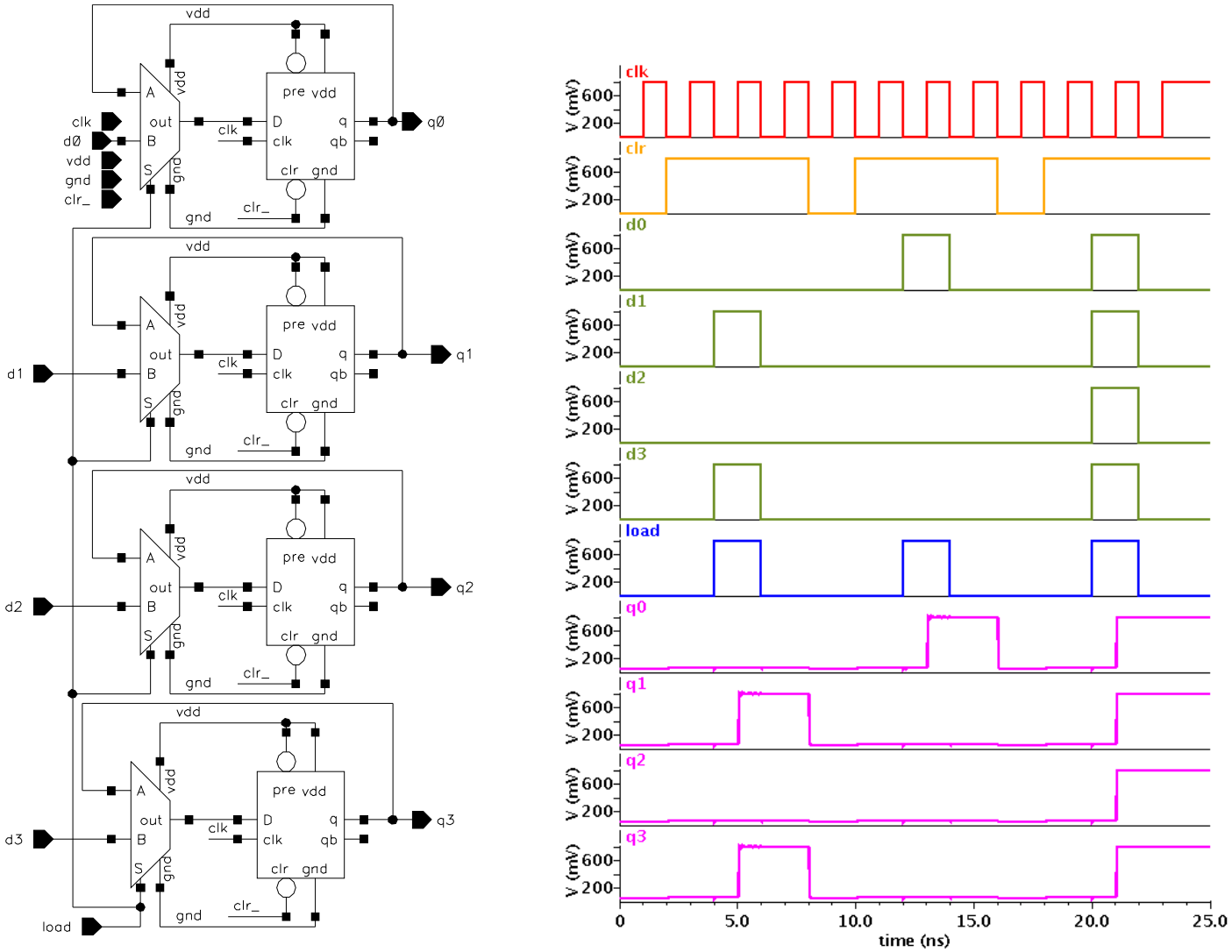


(a) (b)

Figure 3.24: Design of SET based ring counter. (a) Circuit diagram. (b) Transient analysis.

3.5.4 Design of a SET based 4-bit register

The circuit diagram of a SET based 4-bit register is shown in Fig. 3.25(a). The verification of design is carried out using vector file which is listed in Appendix A.4. The transient analysis of 4-bit register is shown in Fig. 3.25(b). The input signals 'clk', 'd(3:0)', 'load'and 'clr' provide inputs as clock, data, load and clear respectively. The 'clr ' clears stored outputs 'q(3:0)' to logic low "0000". The 4-bit register latch 'd(3:0)' to 'q(3:0)' with 'clk'.

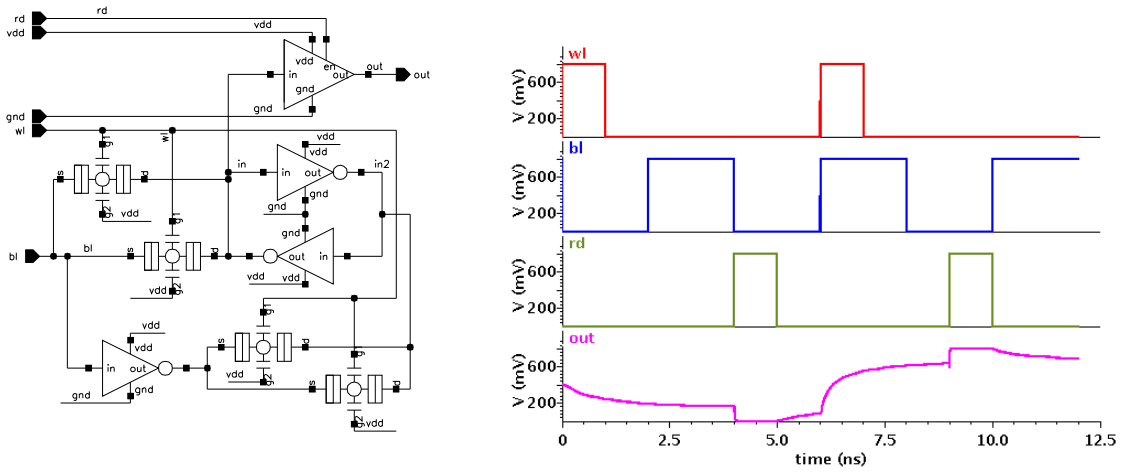


(a) (b)

Figure 3.25: Design of SET based 4-bit register. (a) Circuit diagram. (b) Transient analysis.

3.6 Design of SET based SRAM

The SET based SRAM is used for storage of computer instruction and associated data. The SRAM design is implemented for 16 memory locations and 8-bit data storage. The circuit diagram and transient analysis results of a SET based SRAM cell is shown in Fig. 3.26. The SRAM cell as shown in Fig. 3.26(a) is made up of eight SETs and a tri-state buffer. Each bit in a SRAM cell is stored on two inverters (I0, I1) that are cross-coupled. The two cross-coupled inverters will continue to reinforce each other to retain the data as long as power supply is available. This SRAM cell may have either data of 0 or 1. Four additional access transistors serve to control access over SRAM cell during read and write operations. An SRAM cell has three different states: data writing (updating the SRAM contents), data reading (accessing the stored data) and standby (no change in SRAM contents) mode.



(a) (b)

Figure 3.26: Design of SET based SRAM cell. (a) Circuit diagram. (b) Transient analysis.

The data write to the SRAM cell is accomplished by asserting the word line ('wl'). The 'wl' controls four access transistors (I3, I4, I5 and I6). The I3 and I4 transistors are connected to the bit line 'bl' whereas I5 and I6 transistors are connected to the inverted of bit line 'bl'. So, during write operation ('wl' high state), the available data at 'bl' is stored in SRAM cell. If there is need to store 'X' data then first 'X' is applied at 'bl' which is followed by 'wl' high assertion. This stores data because the bit line input-drivers are designed to be much stronger by connecting two parallel SETs than the relatively weak cross-coupled transistors. So, they can easily override the previous state of the cross-coupled inverters. During read

operation, the read signal 'rd' is actively driven high. This will route the stored data bit to the SRAM cell output through tri-state buffer. During the standby mode (when the 'wl' or 'rd' are not asserted) the access transistors (I3, I4, I5 and I6) disconnect the cell from the bit lines. The transient analysis of SRAM cell is shown in Fig. 3.26(b).

The SET based computing system incorporates 16x8 memory. The block diagram of 16x8 SRAM is shown in Fig. 3.27. The 16x8 memory is structured with the 16 address rows by 8-bit data columns. At the juncture of each of the row and column, an SRAM cell is used to store one data bit information. The 16x8 memory requires 128 SRAM cells. The SRAM cell number nomenclature in the Fig. 3.27 is followed as, first two digits are for row number and last digit is for bit number. For example, the "SRAM cell 146" indicates that this SRAM cell is for 14^{th} row and 6^{th} bit. The 16x8 SRAM uses individual write and read pulse for the access of 8-bit data. The outputs of SRAM cells of each column are connected via tri-state buffers. The transient analysis of 16x8 SRAM is shown in Fig. 3.28. It shows 8 'bl' lines and 8 'out' lines. The Fig. 3.28 shows two times 8-bit data write and read operations for 16 address locations. The data is being wrote sequentially for 16 address through 8 'bl' lines which is sub-sequentially read at 8 'out' lines. It can be seen that the read out data matches completely with write data.

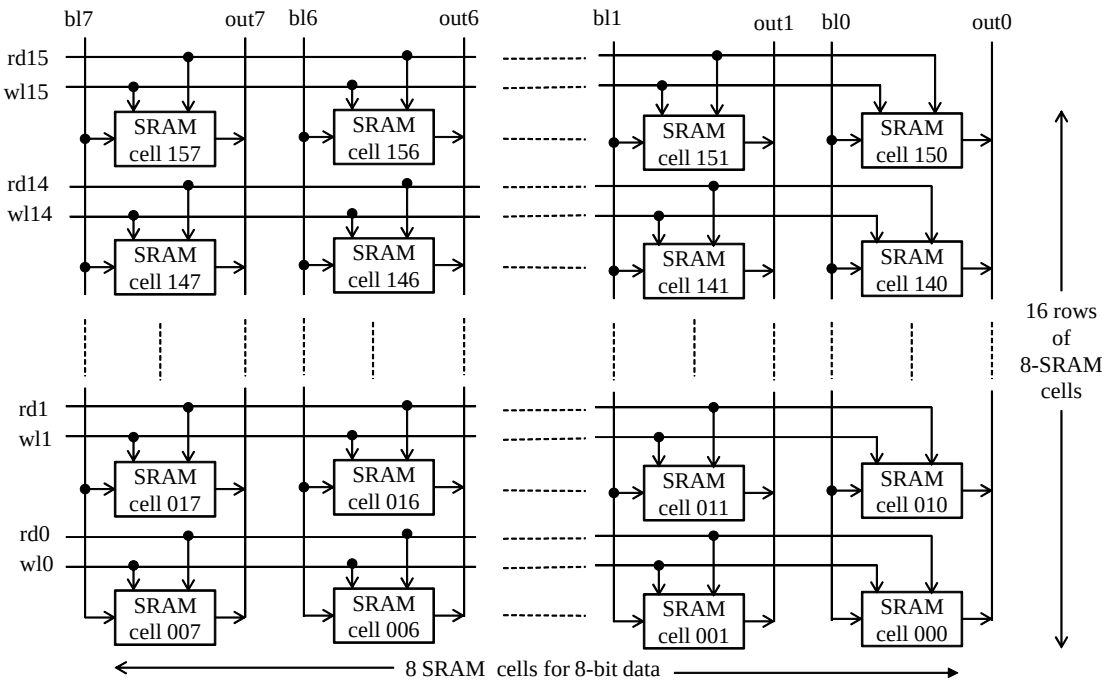


Figure 3.27: Block diagram of 16x8 SRAM.

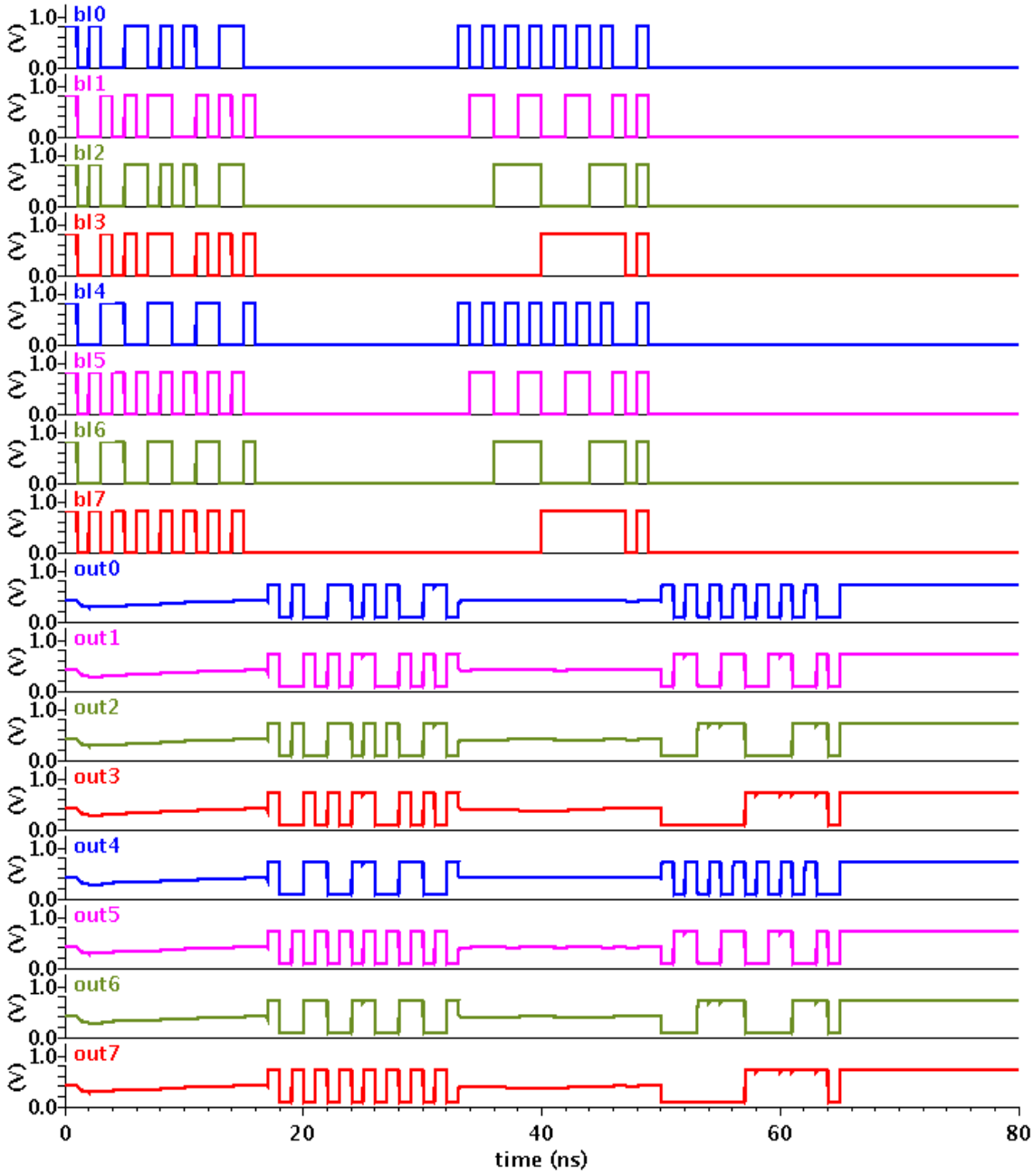


Figure 3.28: Transient analysis of 16x8 SRAM

The detailed data for address location 9 is presented in Fig. 3.29. The transient analysis represents 8-bit write and read data in bus format with the write pulse 'wl9' and read pulse 'rd9'. The figure shows the data access operation for 9^{th} row in Fig. 3.27. The remaining 15 number of individual write and read pulses are not shown in the figure. It can be seen from the Fig. 3.29 that the memory read data 'out[7:0]' follows the stored data as 'bl[7:0]'. The high end conventional memory design with pre-charge and sense amplifier circuit blocks will be incorporated in the future designs.

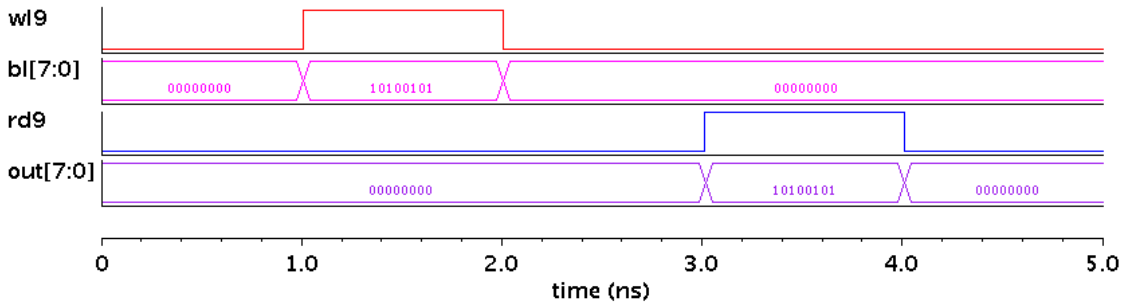


Figure 3.29: Transient analysis of 16x8 SRAM for data access at address location – 9

3.7 Design of SET based controller

The task of a controller is to manage the program execution for the computing system. It is achieved by handling instruction and data flow by individual circuit blocks enabling via control signals. The controller generates 'Cp', 'Ep', 'Lm', 'CE', 'Li', 'Ei', 'La', 'Lb', 'Ea', 'Eu', 'sel_neg', 'sel_op1', 'sel_op2', 'force_carry1', 'carry_prev' and 'mul' signals to the clock ('CLK') and clear ('CLR') signals. These signals are generated with falling edge of clock and used by relevant circuit blocks with the rising edge of the clock to avoid meta-stability. The function of each signal is described as: 'Cp' increments PC; 'Ep' enables PC; 'Lm' loads PC contents to memory address decoder; 'CE' enables memory; 'Li' loads instruction; 'Ei' enables instruction; 'La' loads memory contents to accumulator; 'Lb' loads memory contents to register-B; 'Ea' enables accumulator and 'Eu' outputs the accumulator contents to bus. The remaining signals are used for ALU operation which are described in Section 3.4.1.

The proposed SET based computing system has a fixed length instruction cycle of 6-states which are shown in Fig. 3.27. Table 3.3 shows signal generation during each state. The first 3-states are part of the instruction fetch cycle and remaining belong to the instruction execution cycle. The fetch cycle comprises of address state (T1), PC increment state (T2) and memory state (T3) which are listed as common cycles as in Table 3.3. The fetch cycle is identical for every instruction and henceforth associated signal polarity is also same. The execution cycle consists of instruction decode state (T4), memory read and process state (T5), and data operation state(T6) as per the instruction. The signals during execution cycle depend on the operation performed on the data. The controller manages the signal generation for the entire computing system by their commencement and termination during the instruction execution.

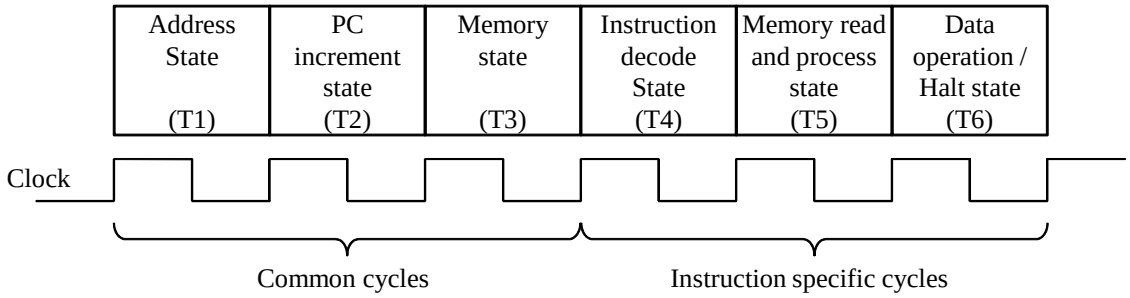


Figure 3.30: Instruction executions states for SET based computing system

The SET based controller comprises of a 6-state ring counter, a 4x16 decoder and combinational gates to generate control signals. The 6-state ring counter generates a pulse of 1 clock cycle width for each state. The generated pulses of ring counter are used in conjunction with instruction decoder outputs. These outputs are decoded by combination gates for controller output signals generation. The design of SET based controller is shown in four circuit diagrams which are detailed in Fig. 3.31 and 3.32. The transient analysis of controller is shown in Fig. 3.33. The associated vector file for verification of controller is listed in Appendix A.5. The vector file generates all opcodes supported by SET based computing system.

3.8 Design of SET based computing system

This section details the SET based computing system design and verification. The previous sections have presented the basic building blocks of SET based computing system these are decoder, multiplexer, tri-state buffers, flip-flop, ring counter, PC, accumulator, register, ALU, 16x8 memory and controller. The block diagram representation of SET based computing system and its interconnections between different sub-blocks are shown in Fig. 3.1 and Fig. 3.34 respectively. The 4-bit counter (Section 3.5.2) is used as PC in the computing system. The 4-bit registers (Section 3.5.4) are used for latch and store intermittent data on the computing system bus. The computing system has total 7 numbers of 4-bit registers namely, a MAR, two each for IR, registers A and B. The design of ALU, controller and 16x8 memory are shown in Sections 3.4, 3.7 and 3.6 respectively. The verification of computing system is carried out with vector files tat is discussed in next chapter.

Table 3.3: Control signals generated by SET based controller

Op-code	Inst.	State	Control Signals																
			Cp	Ep	Lm	Ce	Li	Ei	La	Lb	Eu	Ea	sel_ neg	sel_ op1	sel_ op2	shift_r	force_ carry1	carry_ prev	mul
Cycles		T1	0	1	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0
		T2	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
		T3	0	0	0	1	1	0	0	0	0	0	0	0	1	0	0	0	0
0	LDA	T4	0	0	1	0	0	1	0	0	0	0	0	0	1	0	0	0	0
		T5	0	0	0	1	0	0	1	0	0	0	0	0	1	0	0	0	0
		T6	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
1	LDB	T4	0	0	1	0	0	1	0	0	0	0	0	0	1	0	0	0	0
		T5	0	0	0	1	0	0	0	1	0	0	0	0	1	0	0	0	0
		T6	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
2	MOV	T4	0	0	0	0	0	0	0	1	0	1	0	0	1	0	0	0	0
		T5	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
		T6	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
3	ADD	T4	0	0	1	0	0	1	0	0	0	0	0	0	1	0	0	0	0
		T5	0	0	0	1	0	0	0	1	0	0	0	0	1	0	0	0	0
		T6	0	0	0	0	0	0	1	0	1	0	0	1	0	0	0	1	0

Op-code	Inst.	State	Control Signals															
			Cp	Ep	Lm	Ce	Li	Ei	La	Lb	Eu	Ea	sel_ neg	sel_ op1	sel_ op2	shift_r	force_ carry1	carry_ prev	mul
4	SUB	T4	0	0	1	0	0	1	0	0	0	0	0	0	1	0	0	0	0
		T5	0	0	0	1	0	0	0	1	0	0	0	0	1	0	0	0	0
		T6	0	0	0	0	0	0	1	0	1	0	1	1	0	0	0	0	0
5	ANA	T4	0	0	1	0	0	1	0	0	0	0	0	0	1	0	0	0	0
		T5	0	0	0	1	0	0	0	1	0	0	0	0	1	0	0	0	0
		T6	0	0	0	0	0	0	1	0	1	0	0	1	1	0	1	0	0
6	ORA	T4	0	0	1	0	0	1	0	0	0	0	0	0	1	0	0	0	0
		T5	0	0	0	1	0	0	0	1	0	0	0	0	1	0	0	0	0
		T6	0	0	0	0	0	0	1	0	1	0	0	0	0	0	1	1	0
7	XRA	T4	0	0	1	0	0	1	0	0	0	0	0	0	1	0	0	0	0
		T5	0	0	0	1	0	0	0	1	0	0	0	0	1	0	0	0	0
		T6	0	0	0	0	0	0	1	0	1	0	0	1	0	0	1	1	0
8	CMA	T4	0	0	1	0	0	1	0	0	0	0	0	0	1	0	0	0	0
		T5	0	0	0	1	0	0	0	1	0	0	0	0	1	0	0	0	0
		T6	0	0	0	0	0	0	1	0	1	0	0	1	0	0	1	1	0

Op-code	Inst.	State	Control Signals																
			Cp	Ep	Lm	Ce	Li	Ei	La	Lb	Eu	Ea	sel_ neg	sel_ op1	sel_ op2	shift_r	force_ carry1	carry_ prev	mul
9	RLC	T4	0	0	1	0	0	1	0	0	0	0	0	0	1	0	0	0	0
		T5	0	0	0	0	0	0	0	1	0	1	0	0	1	0	0	0	0
		T6	0	0	0	0	0	0	1	0	1	0	0	1	0	0	0	1	0
A	RRC	T4	0	0	1	0	0	1	0	0	0	0	0	0	1	0	0	0	0
		T5	0	0	0	1	0	0	0	0	1	0	0	0	1	0	0	0	0
		T6	0	0	0	0	0	0	1	0	1	0	0	0	1	1	1	0	0
B	MUL	T4	0	0	1	0	0	1	0	0	0	0	0	0	1	0	0	0	0
		T5	0	0	0	1	0	0	0	1	0	0	0	0	1	0	0	0	0
		T6	0	0	0	0	0	0	1	0	1	0	0	0	1	0	0	0	1
C	OUT	T4	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0
		T5	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
		T6	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
D	NOP	T4	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
		T5	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
		T6	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

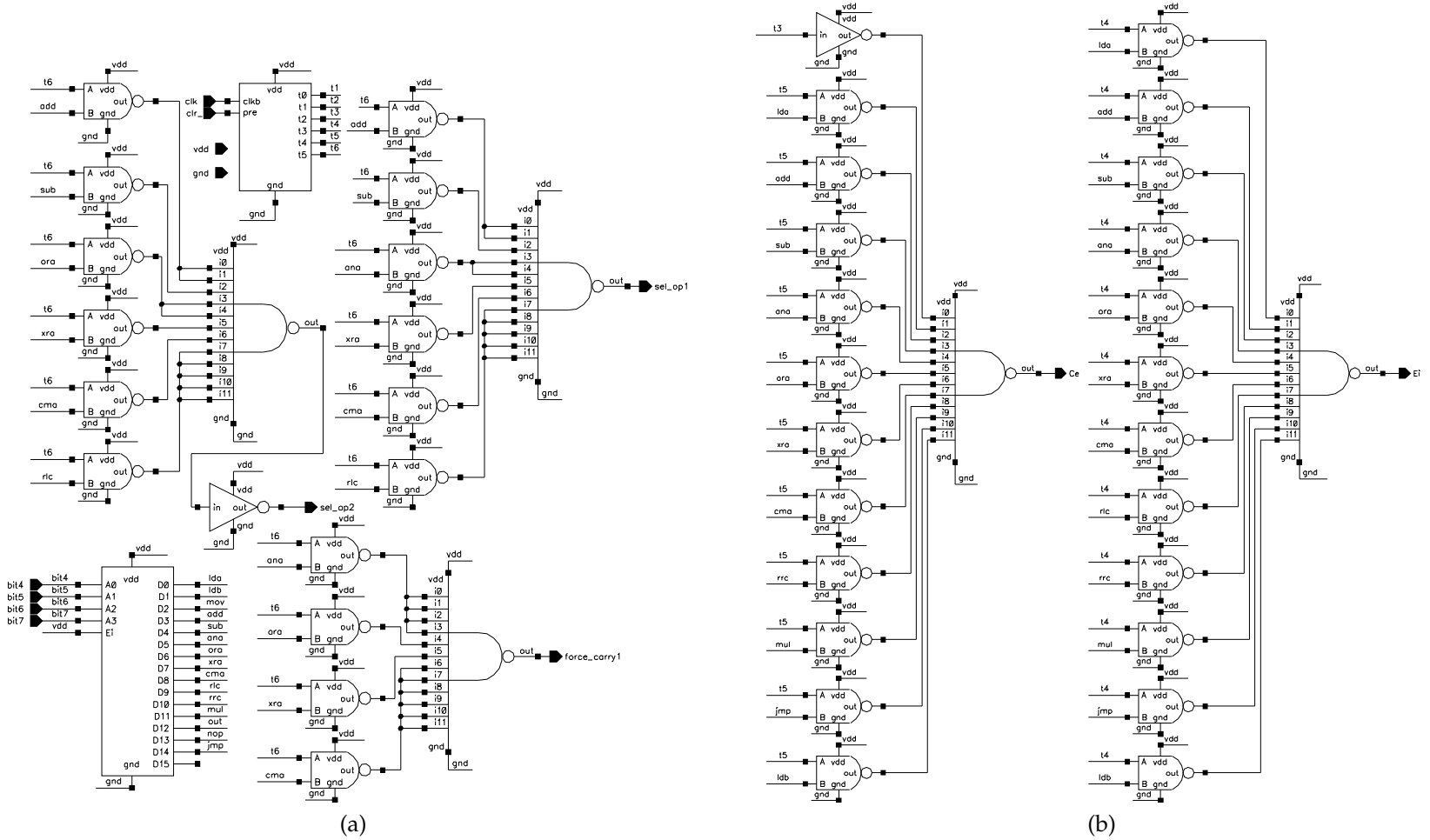


Figure 3.31: Design of SET based controller (cont'd to Fig. 3.32). (a) Part-1. (b) Part-2.

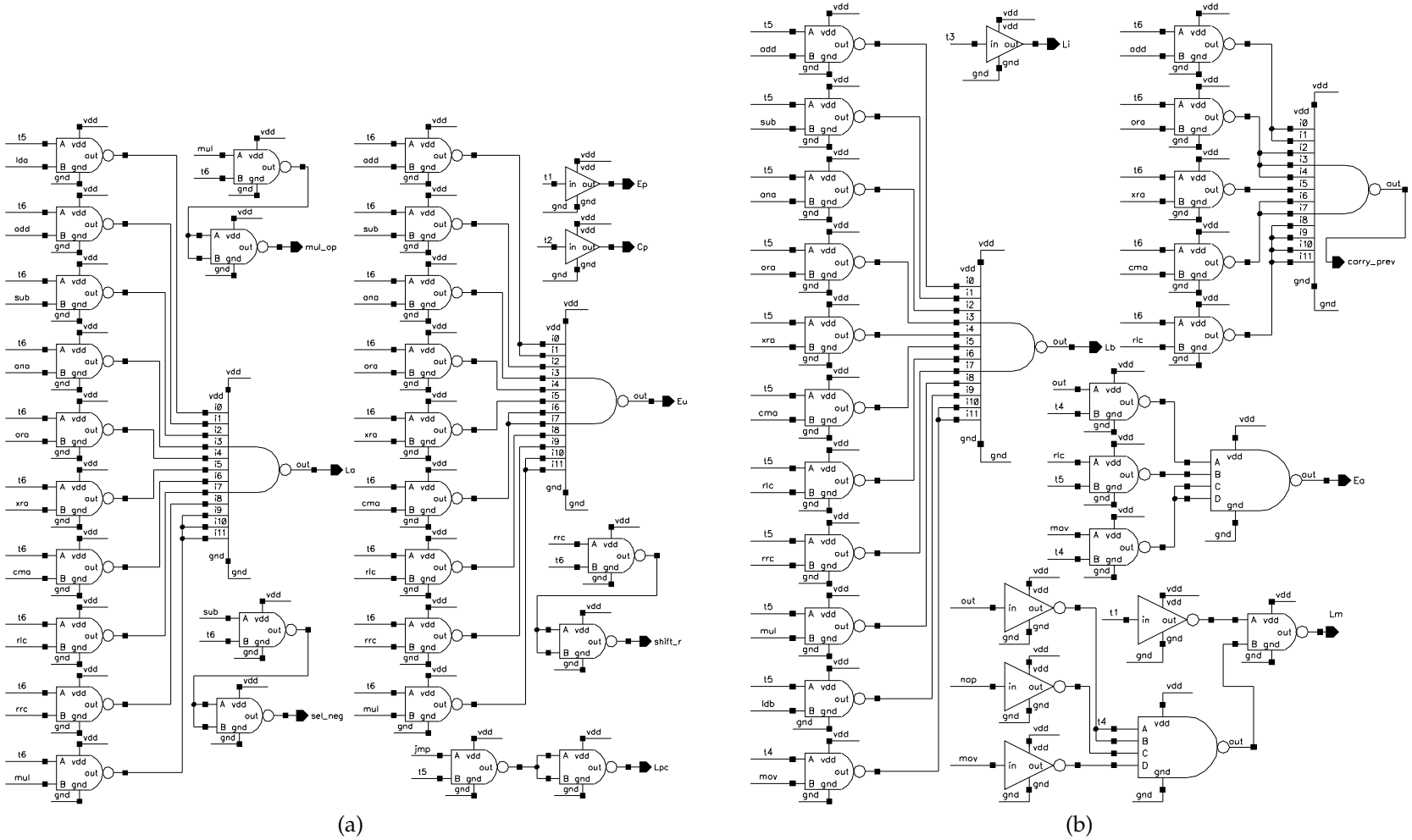


Figure 3.32: Design of SET based controller (cont'd from Fig. 3.31). (a) Part-3. (b) Part-4.

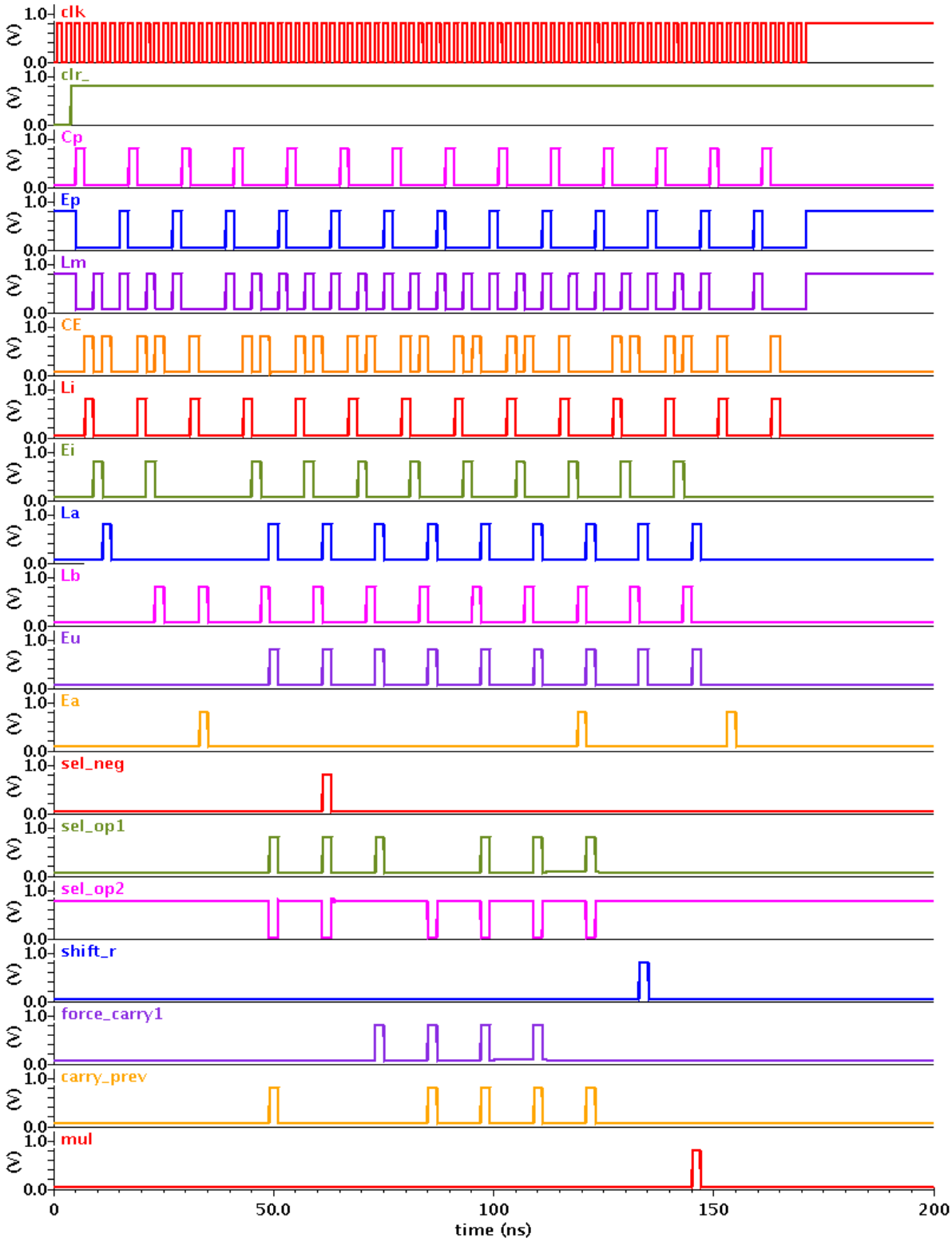


Figure 3.33: Transient analysis of controller.

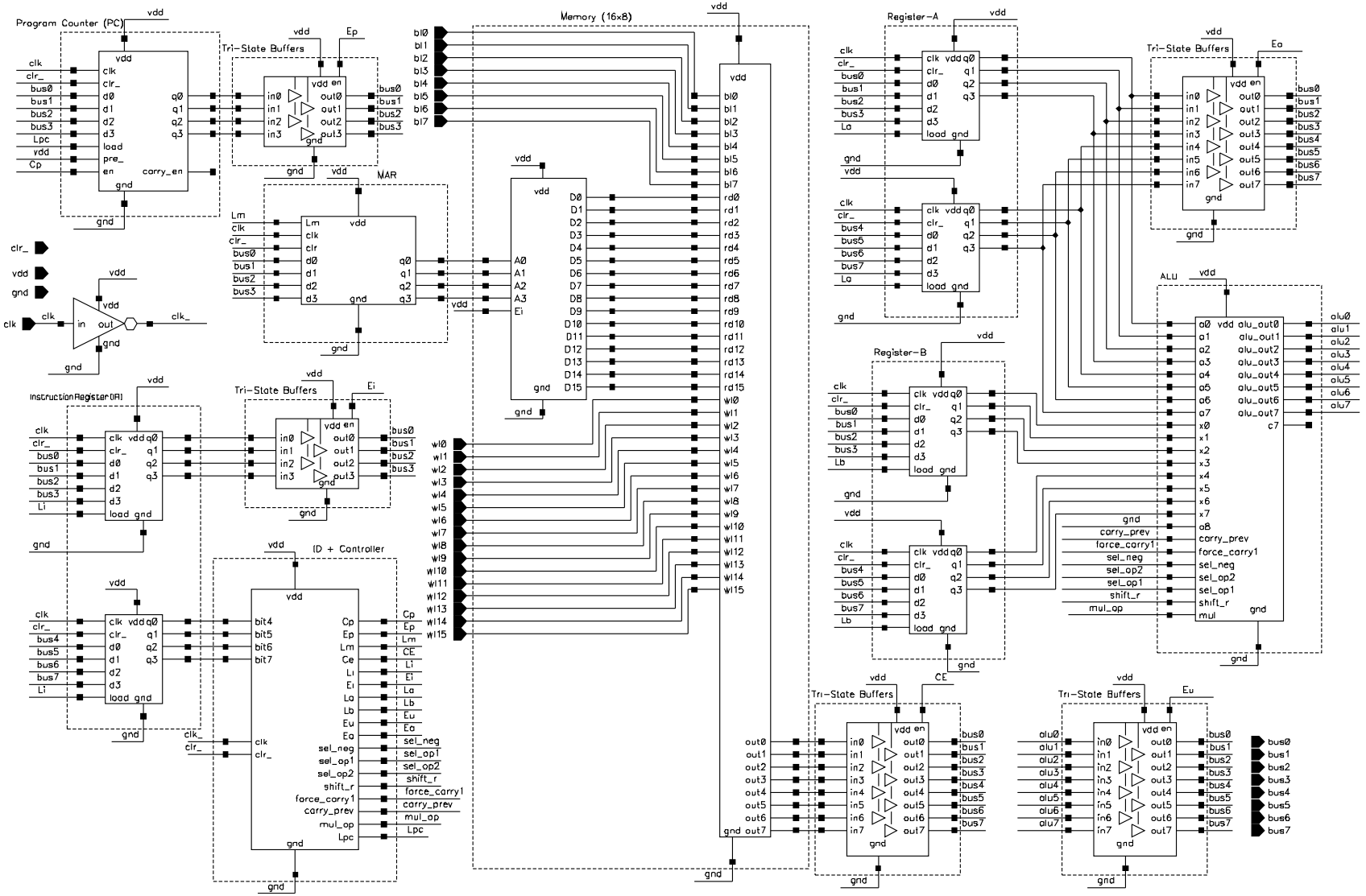


Figure 3.34: Circuit diagram SET based computing system.

CHAPTER 4

Tool Development for Verification of SET Based Computing System.

The SET based circuit designs are verified through individual signal sources connected to each of the circuit inputs with cadence ADE. Each of the signal source has a pattern of repeatable nature of data. This is viable for smaller or block level designs. For large designs like computing systems, this approach is not feasible as there are higher input nodes and complex pattern for each signal type. The SET based computing system requires instruction level simulation and analysis through a defined environment. Such an environment is not readily available for emerging nano-device like SET and complex design as computing system. So, for simulation and analysis of SET based computing system, a tool is developed that accord with core frame-work of Cadence ADE. The developed tool provides peripheral interface and generates input stimuli that is directly compatible to ADE.

4.1 Necessity for tool development

The verification of the computing system requires extensive and complex stimuli. There is no specialized design and simulation software available for SET based computing system. Performing verification through conventional method by assigning individual signal source to each input is not optimum as the number of all possible sets of input combinations are extremely large for computing system. To this front, Cadence ADE magnificently provides the flexibility to simulate the design using a vector file.

A vector file consists of IO vectors (signals); their voltage levels, time interval, rise time, fall time and their transition information. The vector file consists of input vectors (signals) that are to be applied to the system inputs during the verification. These vectors are executed sequentially based on the time interval defined in the vector file. The computing

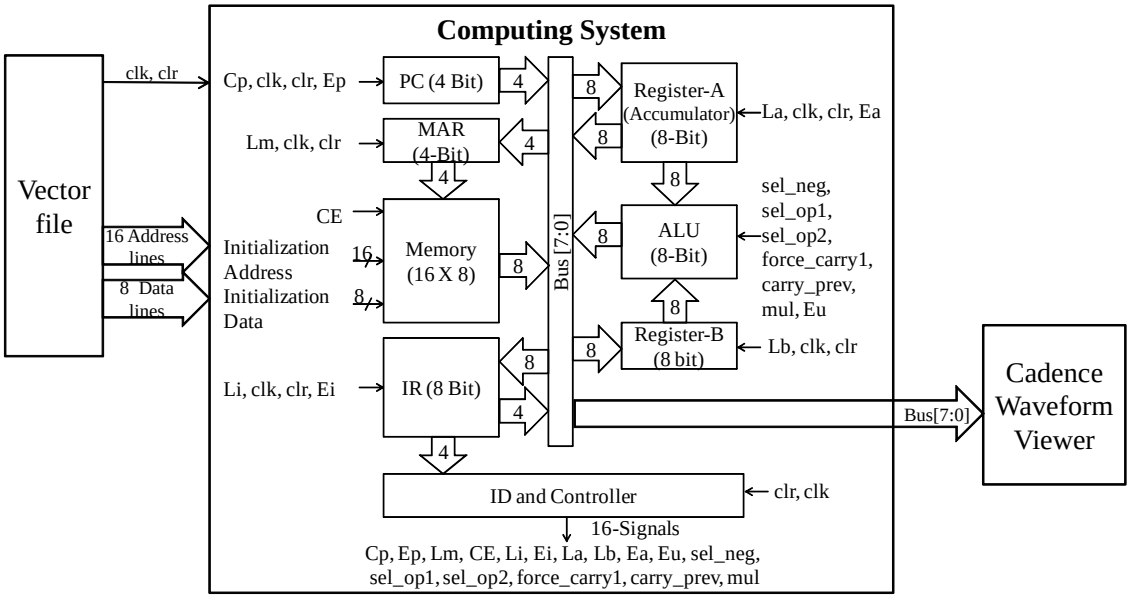


Figure 4.1: Block diagram for computing system verification. Vector file generates stimuli to computing system and Cadence waveform viewer shows I/O signals

system needs large number of IO signals which are generated through the vector file and defining vector file manually is bulky, erroneous and complex. This hassle can be solved by generating the vector file by a tool for user-defined instructions and parameters. In order to overcome this problem, we have designed and developed a graphical user interface (GUI) based tool that accepts user given instructions and translates it to a vector file using Microsoft Visual Basic-5.0. In absence of such a tool, the simulation of SET based computing system is difficult at assembly code level.

The block diagram for SET based computing system verification is shown in Fig. 4.1. The computing system has 16 word lines as 'wl(0:15)', 8 data lines as 'bl(7:0)', 'clk' and 'clr' input signals. The output of computing system is available on 'Bus [7:0]'. The input word lines and data lines stores user selected data into the 16x8 SRAM. These data is read with respect to 'clk' and 'clr' signals.

4.2 Architecture of tool

The vector file generation tool consists of four frames namely, 'Program' frame, 'Computer memory' frame, 'Accumulator data' frame and 'Timing and voltage parameters' frame. The 'Program' frame provides the instruction set support for the SET based computing system and user data selection facility. The 'Computer memory' frame lists selected

instructions with its hexadecimal converted information that are to be stored in 16x8 memory of the computing system. The 'Accumulator data' frame displays accumulator content after execution of user selected instructions. Fig. 4.2 shows the GUI of the program after selecting the sample instructions code as shown in Table 4.1. Fig. 4.2 shows the expected accumulator data after execution of sample code that can be verified during the verification. The 'Timing and voltage parameters' frame allows user to edit the timing parameters which are a part of vector file. In the present case of the computing system, the vector file includes signals definition, initialization sequence and clock generation. The initialization sequence contains op-codes and data for user-defined instructions.

Table 4.1: Sample code for SET based computing system

LDB, 1E :	Load register-B with content of 1E
LDA, 89 :	Load Accumulator with content of 89
ANA, 0F :	AND 0F with Accumulator
MUL, 0A :	Multiply Accumulator (Lower Nibble) with A
NOP, 0A :	No operation
RLC, FF :	Shift Left the content of Accumulator
CMA, FF :	Complement the content of Accumulator
OUT, 0A :	Output the content of Accumulator

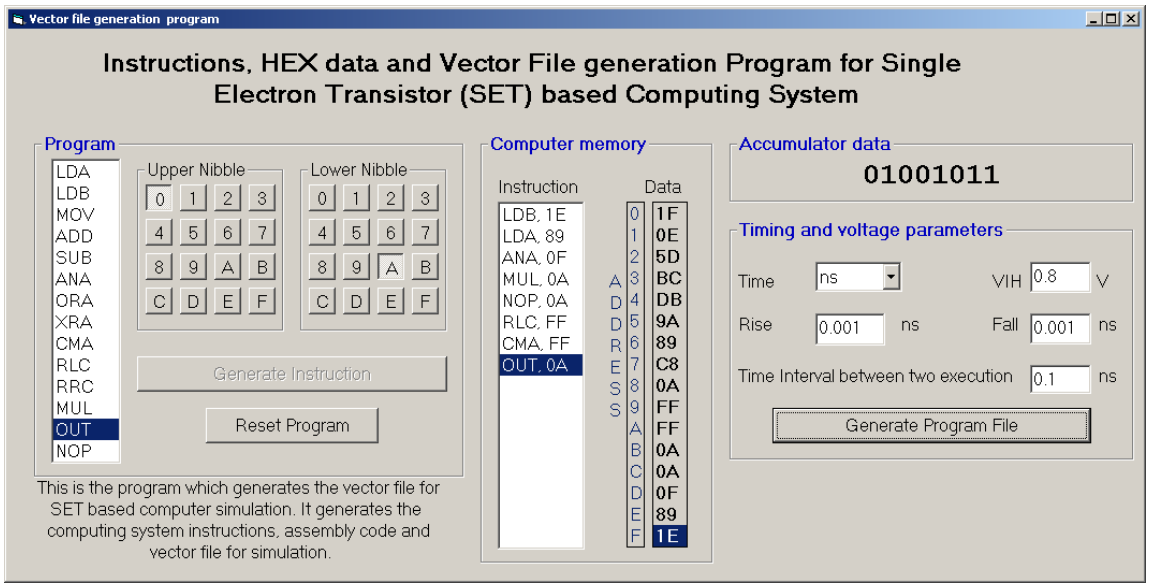


Figure 4.2: A snapshot (GUI) of test-bench generation tool.

I The 'Program' frame list out the SET based computing system supported instructions and data. The computing system machine code has two nibbles: an upper and a lower nibble. The upper nibble represents instruction code whereas lower nibble shows address pointer of the operand. The program frame contains two command buttons, one is 'Generate Instruction' and other is 'Reset Program'. The 'Generate Instruction' command button execution creates an instruction and lists in the adjacent list box in GUI. The execution of 'Reset Program' command button resets the tool to initial state. The SET computing system has 16 memory locations and it requires two memory locations for storage of each instruction. The SET computing system memory comes to be full after eight instructions. Hence, the tool disables Generate Instruction command button automatically.

II The 'Computer Memory' frame has two list boxes. One shows user selected instruction and other shows data stored in the memory of the computing system. The instruction list box appends on each 'Generate Instruction' execution. The data list to address (in 'Computer Memory' frame) shows the data at each memory address of computing system. 'Generate Instruction' command button execution reloads the instruction and data list boxes.

III The 'Accumulator Data' frame displays the expected accumulator contents of the computing system after execution of current instruction. This data is useful during waveform viewing.

IV The 'Timing and voltage parameters' frame consists time unit, high voltage level, time interval, rise time and fall time parameters. Cadence spectre simulator uses this information during run time simulation. The time interval is the read out rate of between to consecutive samples of vector file. The rise and fall time are applied during transition of each signal. The execution of 'Generate Program File' command button produces the vector file for user-selected instructions along with timing parameters.

In the case of computing system; the vector file has signals definition, initialization sequence and clock generation. The initialization sequence contains op-codes and data for user defined instructions which are stored in 16 X 8 memory. Later on, the same memory locations are read out during simulation. The salient features of the program are as below:

- It has the instruction set support for SET based computing system.

- It allows users to select the instruction and data as per the requirement.
- The generated instructions are displayed in the list.
- During each instruction generation the accumulator contents are displayed on screen.
- The program automatically manages memory addresses locations when no data operand is required for CMA, NOP, RLC, RRC and OUT instructions.
- The program can be made reset at any time.
- The program has timing parameter information editing facility which allows the user to change time scale, rise time, fall time and level of signals.
- It displays when the output will be available on the simulation for OUT instruction.

4.3 Tool code execution

The Fig. 4.3 shows a flow chart of the program execution. At the starting of the program, the 'Program' frame is initialized with list of instruction codes, the 'Computer memory' frame with an empty instruction list and all memory data with 0x00, the 'Accumulator Data' frame with '00000000' data and the 'Timing Parameter' frame with default timing parameters. Also, the run time variables are initialized to their default values. It is referred as initialization state. The tool source code is attached in Appendix-B.

On executing *Generate Instruction* command, the program does four tasks for instruction generation and 'Computer memory' frame update.

I It generates the mnemonic by concatenating the instruction with selected data nibbles. It updates the mnemonic to 'Computer memory' frame instruction list box.

II It determines the address location for current instruction machine code and address pointer where relevant operand are to be stored. The program finds out the address pointer based on previous instruction completion.

III It reads the user selected instruction and determine opcode from the stored look-up table. Based on this information, it generates the machine code and writes to the 'Computer memory' frame data list box.

IV It writes the operand at the determined address pointer in the 'Computer memory' frame data list box.

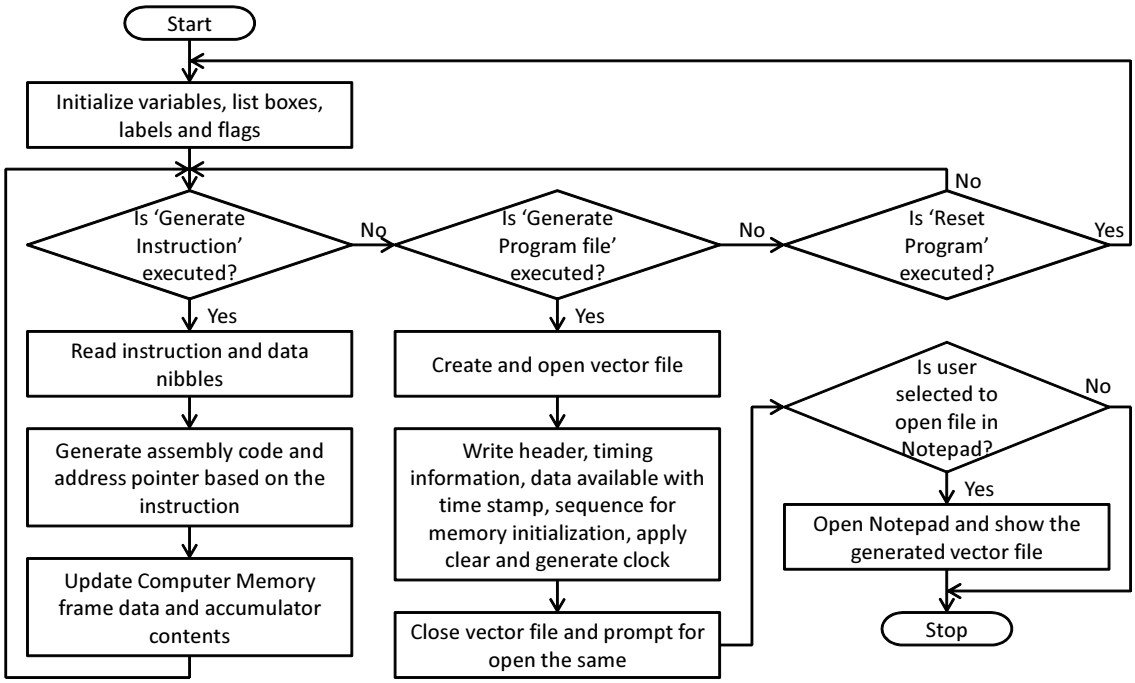


Figure 4.3: A flow chart of program execution.

On executing *Generate Instruction* command, the program does two tasks for 'Accumulator Data' frame update.

I The program has 'ADD', 'SUB', 'ANA', 'ORA', 'XRA', 'CMA', 'RLC', 'RRC' and 'MUL' subroutines for calculating the accumulator content after instruction execution. These subroutines are called based on selected instruction.

II Each of this subroutine process the supplied data as parameter and returns the calculated value. This value is updated in the 'Accumulator data' frame.

On executing *Generate Program file* command, the program generates vector file which consists four sections: 1) file header, 2) signal declaration with timing information and output occurrence during verification of 'OUT' instruction 3) memory initialization and 4) clear and clock generation. The generated vector file for sample code as per Table-4.1 is shown in Fig. 4.4.

1. The file header shows the institute names and system date/time information as comments. The line with comment starts with ; in vector file.

2. Each of the signal is declared with their radix, names and type in the beginning of a vector file. It also includes the timing information for these signals. The timing information lists time unit, rise time, fall time and period. The period defines

```
; -----------        BC 0008 1 0         00 0000 1 0         00 0000 1 1         00 0000 1 0
; Vector file for    DB 0010 1 0         ; -----------       00 0000 1 0         00 0000 1 1
; SET based          9A 0020 1 0         ; LDA, 89           00 0000 1 1         00 0000 1 0
;Computing System    89 0040 1 0         00 0000 1 1         00 0000 1 0         00 0000 1 1
;Testing             C8 0080 1 0         00 0000 1 0         00 0000 1 1         00 0000 1 0
;     Date: 12-      0A 0100 1 0         00 0000 1 1         00 0000 1 0         ; -----------
;04-2019 Time:       FF 0200 1 0         00 0000 1 0         00 0000 1 1         ; CMA, FF
;09:44:38 PM         FF 0400 1 0         00 0000 1 1         00 0000 1 0         00 0000 1 1
;     Generated      0A 0800 1 0         00 0000 1 0         00 0000 1 1         00 0000 1 0
;from VB Program     0A 1000 1 0         00 0000 1 1         00 0000 1 0         00 0000 1 1
;          SAC /     0F 2000 1 0         00 0000 1 0         ; -----------       00 0000 1 0
;DAIICT              89 4000 1 0         00 0000 1 1         ; NOP, 0A           00 0000 1 1
;     Ahmedabad /    1E 8000 1 0         00 0000 1 0         00 0000 1 1         00 0000 1 0
;Gandhinagar         ; -----------       00 0000 1 1         00 0000 1 0         00 0000 1 1
; -----------        ;Config OVER; uP    00 0000 1 0         00 0000 1 1         00 0000 1 0
RADIX 44 4444 1 1    ;Reset Start        ; -----------       00 0000 1 0         00 0000 1 1
vname bl[7:0]        00 0000 0 1         ; ANA, 0F           00 0000 1 1         00 0000 1 0
wl[15:0] clr clk     00 0000 0 0         00 0000 1 1         00 0000 1 0         00 0000 1 1
IO II IIII I I       ;uP is Reset;       00 0000 1 0         00 0000 1 1         00 0000 1 0
TUNIT ns             ;Program in RUN     00 0000 1 1         00 0000 1 0         ; -----------
TRISE 0.001          ; -----------       00 0000 1 0         00 0000 1 1         ; OUT, 0A
TFALL 0.001          ; LDB, 1E           00 0000 1 1         00 0000 1 0         00 0000 1 1
PERIOD 0.1           00 0000 1 1         00 0000 1 0         00 0000 1 1         00 0000 1 0
VIH 0.8              00 0000 1 0         00 0000 1 1         00 0000 1 0         00 0000 1 1
; -----------       00 0000 1 1         00 0000 1 0         ; -----------       00 0000 1 0
;The output          00 0000 1 0         00 0000 1 1         ; RLC, FF           00 0000 1 1
;01001011 is         00 0000 1 1         00 0000 1 0         00 0000 1 1         00 0000 1 0
;available at        00 0000 1 0         00 0000 1 1         00 0000 1 0         00 0000 1 1
;10.8ns              00 0000 1 1         00 0000 1 0         00 0000 1 1         00 0000 1 0
; -----------       00 0000 1 0         ; -----------       00 0000 1 0         00 0000 1 1
1F 0001 1 0          00 0000 1 1         ; MUL, 0A           00 0000 1 1         00 0000 1 0
0E 0002 1 0          00 0000 1 0         00 0000 1 1         00 0000 1 0         00 0000 1 1
5D 0004 1 0          00 0000 1 1         00 0000 1 0         00 0000 1 1         00 0000 1 0
```

Figure 4.4: A vector file generated by the program.

execution of each line which is 1 ns for the present case. This timing information will be used by the Cadence Spectre tool during the verification. The expected output on the computing system bus with time is denoted in the file as comment.

3. The next section is the memory initialization of the computing system which is based on user selected instructions. The program read each address location from 'Computer memory' frame and add in the vector file with relevant signals.

4. The last section of vector file is the clear and clock signals' generation. The clear is generated for 1 clock cycle. After clear signal generation, the clock is generated for selected instructions by maintaining consecutive 1 and 0 for each line in the vector file. So, the clock cycle time is 0.2 ns for time interval of 0.1 ns. In the SET computing system, each instruction is processed with six clock cycles. Hence, this program generates 6 clocks *i.e.* 12 lines/instruction in the vector file.

On executing *Reset program* command, the program clears the previously stored instructions, relevant data and restore the program to initialization state.

4.4 Transient analysis of SET based computing system

The transient analysis of SET based computing system for the sample code (Table 4.1) execution at the operating frequency of 5 GHz is shown in Fig. 4.5. The input signals of the computing system ('wl(0:15)', 8 data lines as 'bl(7:0)'and 'clr') are not shown in the figure. The output of computing system on 'Bus [7:0]' is shown with the input signal 'clk'. It shows that the binary resultant output data value of 01001011 is available at 10.8 ns with a vertical marker that matches with 'Accumulator data' frame data of Fig. 4.2. The transient analysis of Fig. 4.5 have inferior rise and fall times because of the computing system bus is connected through the tri-state buffers. In the present work, practical interconnect parasitic capacitance at each design node have been incorporated that have been not considered in most of the previous work reported till date as per Table 2.2. It is further analyzed that, the SET based computing system works at higher frequency at lower parasitic node capacitance values.

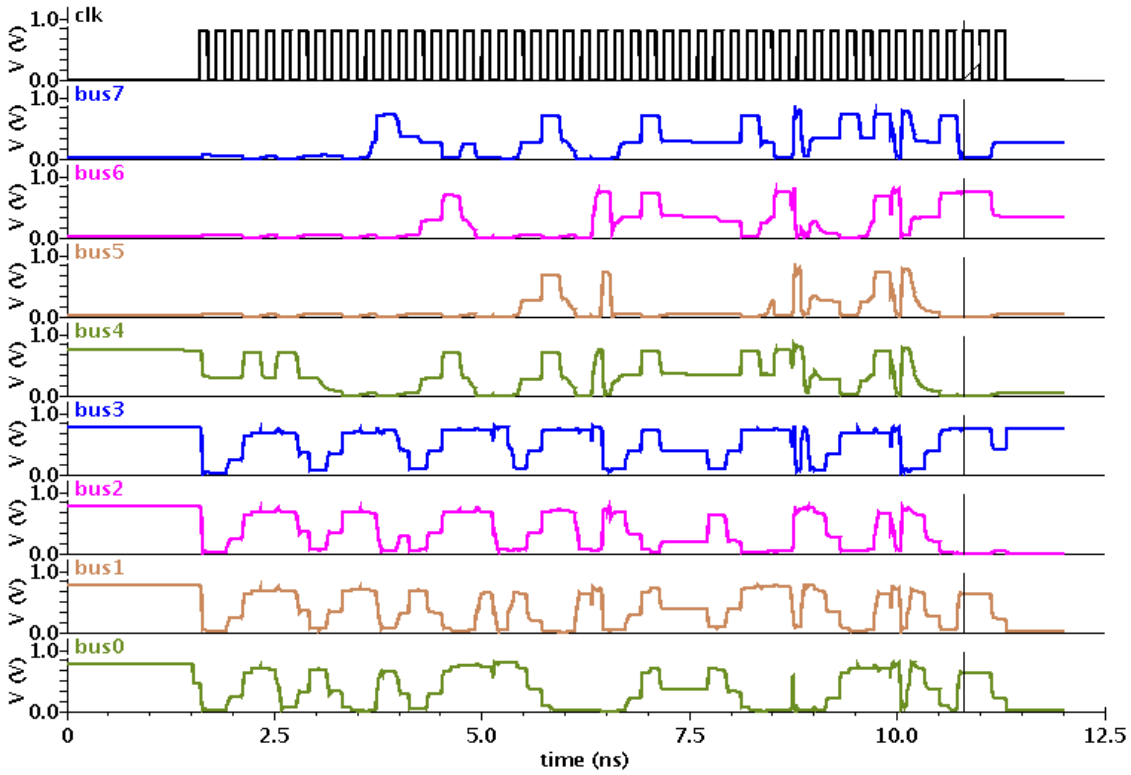


Figure 4.5: Transient analysis of SET based computing system.

CHAPTER 5

Results and Analysis

This section presents various simulation results and performance analyses of SET based circuits as described in the previous sections. Firstly, the formulated analytical model is verified with the simulated results. This is shown in Section 5.1. Thereafter, performance of computing system using prominent SET device is compared with the 16 nm CMOS device. It is investigated that the SET based computing system performs magnificently better than 16 nm CMOS based computing system. Once, establishing and investigating the higher performance of SET, the other design blocks using SET is analyzed in detail. Performance parameters viz. delay and average power dissipation of each of the computing system is obtained and analyzed. The robustness and immunity to variability of SET based system is tested for process, voltage and temperature fluctuations in Section 5.6.

5.1 Performance evaluation of SET device using analytical and simulation models

In the proposed work, we have implemented a SET based computing system. The design follows bottom-up approach using a SET Verilog-A MIB model [10]. The proposed design consists of more than 6000 transistors. The design is implementation and simulation is carried out in Cadence Virtuoso tool set. Since, this kind of SET based large design is not implemented previously, it was sought to have analytical modelling comparison using another tool like, MATLAB. So, we have characterize the same model using analytical and simulation modelling using MATLAB and Cadence Virtuoso tool set respectively. The analytical modelling for characteristics measurements of NSET and PSET is formulated. The I_{ds}–V_{ds} characteristics are determined for five different values of V_{gs}. The flow chart for determining I_{ds}–V_{ds} characteristics using analytical modeling is shown in Figs. 5.1.

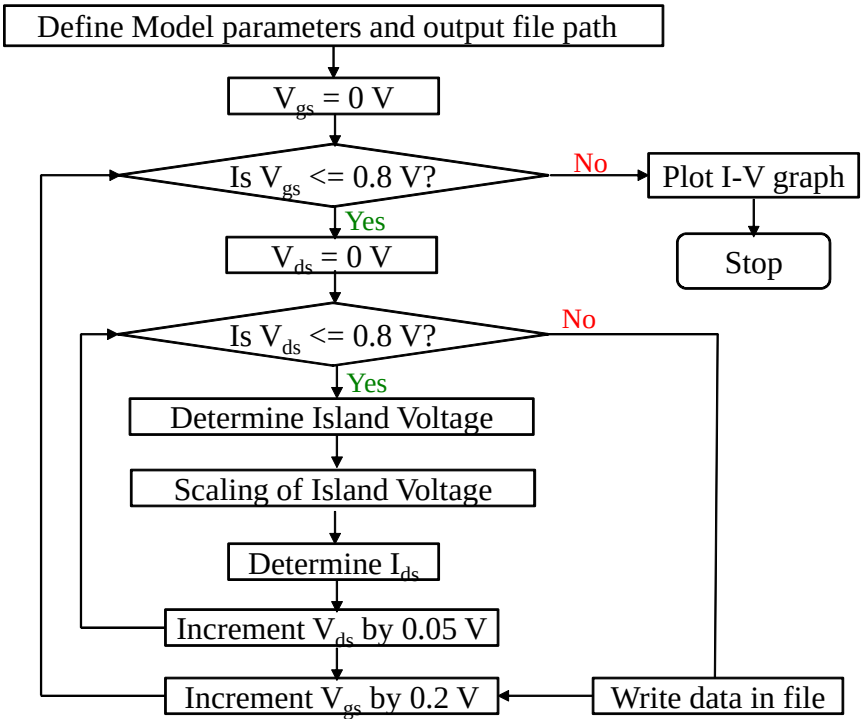


Figure 5.1: The flow chart of SET analytical measurements.

The analytical model is verified with the simulation model that comprises of MIB model in Cadence Virtuoso. Figs. 5.2 and 5.3 represent I_{ds}–V_{ds} characteristics for N-type and P-type SETs respectively. In the figure, 'A' represents the analytical model while 'S' denotes the simulation model results. From the figure, it can be observed that the formulated analytical model results match very closely with the simulation model results. The average percentage error between two models is nearly ±10%.

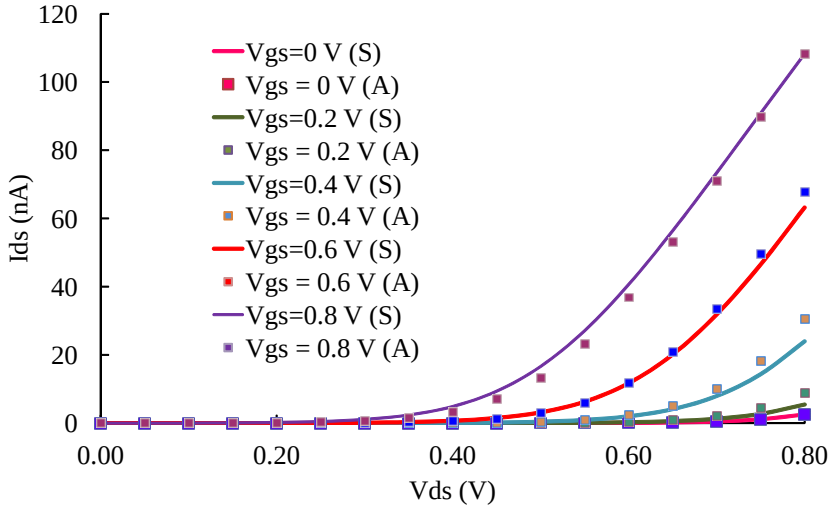


Figure 5.2: The N-type SET I-V characteristics measurements.

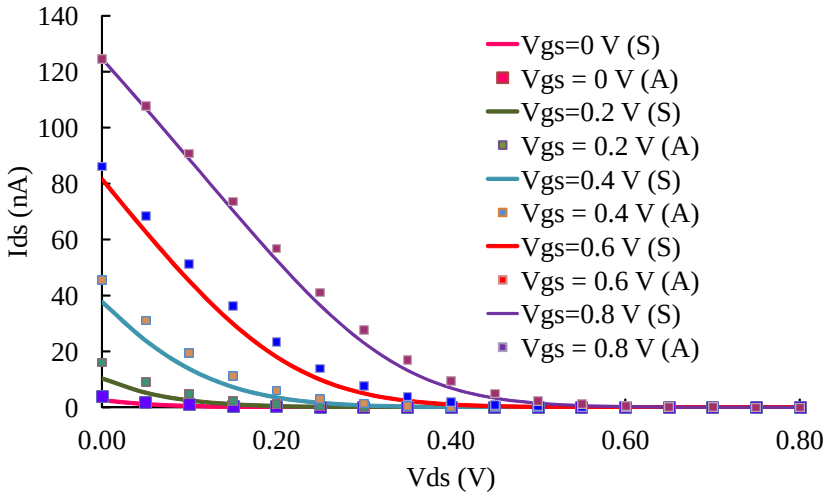


Figure 5.3: The P-type SET I-V characteristics measurements.

5.2 Performance measurement of SET and 16 nm CMOS based circuit blocks

In this section, different components of SET based computing system are analyzed. The circuit diagram, test bench model and functional outputs have been already discussed and presented in Chapter 3. The results of delay and power measurements of SET and 16 nm CMOS based circuits blocks are reported in Table 5.1. The results shows that SET based circuits have better delay and power measurements. The maximum delay derives the operating frequency of the system while average power dissipation in the system reflects the maximum heat generated and associated heat sink requirements. It is analyzed that the maximum delay and power dissipation occurs in the controller circuits. This is because it uses maximum number of combinational elements and does maximum switching over the execution. Hence, future work can be put in to optimize controller circuit for getting smaller delay and power dissipation.

Table 5.1: SET and 16 nm CMOS based components delay and power measurements

Technology	SET		16nm CMOS	
Design block	Delay (ps)	Power (nW)	Delay (ps)	Power (nW)
Inverter	1.02	0.73	3.4	9.5
2-inputs NAND gate	7.37	1.1	14.85	19.9
2-inputs NOR gate	7.13	1.1	26.72	17.9

Technology	SET		16nm CMOS	
Design block	Delay (ps)	Power (nW)	Delay (ps)	Power (nW)
2-inputs XOR gate	10.73	4.9	59.77	54.91
Tri-state buffer	10.01	8.7	36.08	41.92
Full adder	21.11	11.77	101.2	189.6
D-Flip Flop	38.87	7.19	99.73	91.13
4-bit counter	64.82	94.66	184.9	713.3
Ring counter	52.64	41.81	171	557.9
4-bit register	19.64	58.76	105.2	577.4
ALU slice	42.08	23.38	225	249.9
Multiplier	58.08	185.3	207.6	1026
Controller	106.7	213.6	450.9	1208
SRAM cell	9.04	28.57	24.88	353.8

5.3 Performance comparison of SET based logic blocks with previous works

In this section, results of proposed SET based logic blocks are compared with previous published works. During the comparison, only SET based designs are considered and other hybrid designs are avoided. The delay, power, I/O voltage and operating temperature are compared and listed in Table 5.2. It is analyzed that the major design blocks of proposed system gives better results in terms of delay and power. The result at Sr. No. 1, shows better delay than proposed work that is due to in [66], R. Shah *et al.* have proposed buffer design for 22 nm CMOS compatible SET parameters, the single gate SET model usage and 0.55 V switching threshold. The few of the proposed design blocks lags the performance with previous work. That is due to working of previous designs at lower operating temperature and voltages. Also, these do not consider the realistic SET parameters for room temperature operations and interconnect parasitics.

Table 5.2: Results comparison of different SET based components with previous work

Sr. No.	SET based design block	Results from proposed work I/O voltage (V) = 0.8/0.8 V Temperature = 300 K With fabricated SET parameters			Results from SET based previous design works					
		Delay (ps)	Power (nW)	Remark	Ref.	Delay (ps)	Power (nW)	I/O voltage (V)	Temp.	Remark
1	Buffer	0.328	3.65	Without interconnect parasitics	[66]	0.065	25.99	0.8/0.8	300 K	SET parameters compatible to 22 nm CMOS technology
2	Buffer with 20 aF C_L	109.8	4.76		[66]	787.9	26.81	0.8/0.8	300 K	
3	Inverter	1.02	0.73	With interconnect parasitics	[105]	-	0.09	0.05/ 0.017	30 K	Without consideration of realistic SET parameters and interconnect parasitics
4	2-inputs NAND gate	7.37	1.1		[68]	1.29 us	63.7 pW	0.8/ 0.018	300 K	
5	3-inputs NAND gate	18.16	1.6		[60]	33	1.1	0.4/0.4	300 K	
6	2-inputs NOR gate	7.13	1.1		[68]	1.1 us	111 pW	0.8/ 0.015	300 K	
7	3-inputs NOR gate	18.65	1.42		[60]	32.6	0.98	0.4/0.4	300 K	
8	2-inputs XOR gate	10.73	4.9		[60]	14.8	2.47	0.4/0.4	300 K	
9	2x1 multiplexer	21.67	5.32		[60]	0.24	1.97	0.4/0.4	300 K	
10	2x4 decoder	9.68	6.46		[60]	10.8	3.67	0.4/0.4	300 K	
11	D-Flip Flop	38.87	7.19		[60]	12.3	11.8	0.4/0.4	300 K	
12	4-bit register	19.64	58.76		[110]	-	85.3 pW	0.016/ 0.016	-	

5.4 Transient analysis of SET and 16 nm CMOS computing systems

To measure the efficiency of SET based computing system, a 16 nm CMOS based computing system is also designed. The 16 nm CMOS technology based computing system is designed using the same method as with SET based circuit design in Cadence Virtuoso tool-set. Both the systems are analyzed using a vector file that has same code execution as shown in Table 5.3.

Table 5.3: Sample code for SET based computing system

LDA, 59 :	Load Accumulator with content of 59
ADD, 95 :	Add 95 to Accumulator
SUB, A1 :	Subtract A1 from Accumulator
RRC, A1 :	Shift Right the content of Accumulator
CMA, FF :	Complement the content of Accumulator
XRA, 54 :	XOR 54 with Accumulator
ORA, CD :	OR CD with Accumulator
OUT, CD :	Output the content of Accumulator

The GUI for vector file generation for this code for SET based computing system is shown in Fig. 5.4. The generated vector file is listed in Appendix A.6. SET and 16nm CMOS based designs are simulated using the same stimuli. The vector file generates stimuli for 8 different instructions (Table 5.3). During the first 1.6 ns (Appendix A.6 and Fig. 5.4), the data for these instructions is stored in SRAM that is processed when the clock is applied to the computing system. The design architecture executes each instruction in 6 clock cycles. The vector file shows that the bus (7:0) output of "11001101" is available at 10.8 ns. The timing analysis results for the code is shown in Fig. 5.5. It confirms output availability at 10.8 ns with vertical marker for 5 GHz operating frequency.

The GUI for vector file generation for 16 nm CMOS based computing system is shown in Fig. 5.6. It has operating frequency of 1 GHz and the changes in vector file are shown with blue colored text (Appendix A.6). The timing analysis results for the code is shown in Fig. 5.7. It confirms bus (7:0) output of "11001101" available at 54 ns with vertical marker for 1 GHz operating frequency. The 16 nm CMOS based computing system operation is limited by inherent device capacitance.

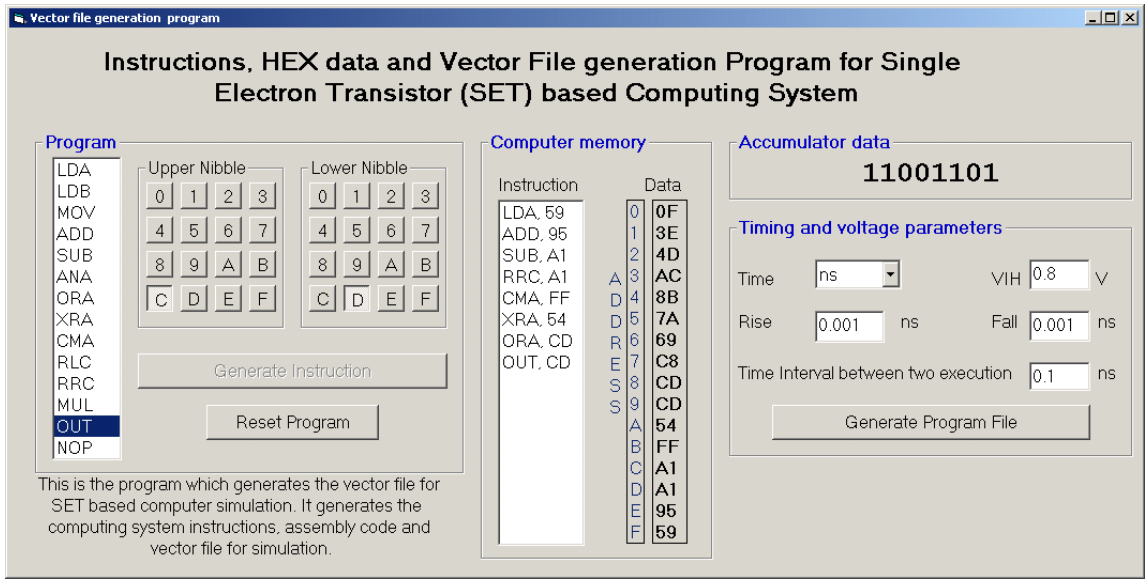


Figure 5.4: The GUI of vector file generation of code for SET based computing system.

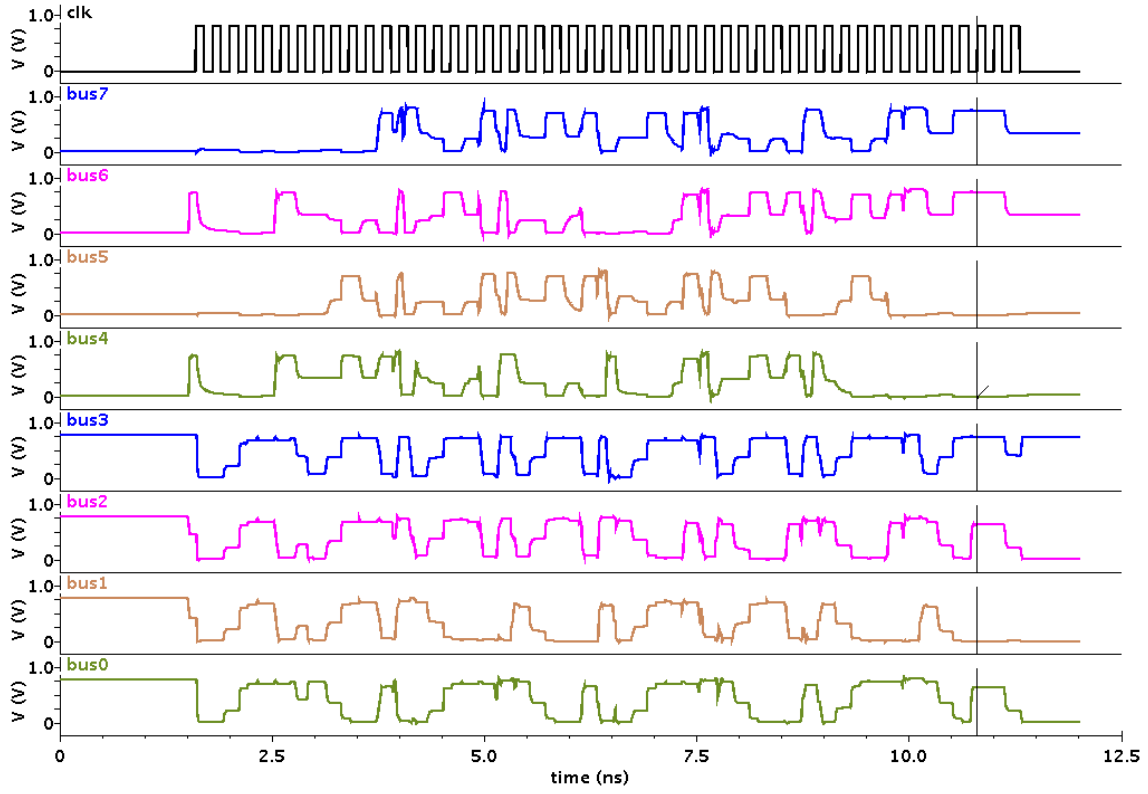


Figure 5.5: The transient analysis of SET based computing system at 5 GHz for instructions as per Table 5.3.

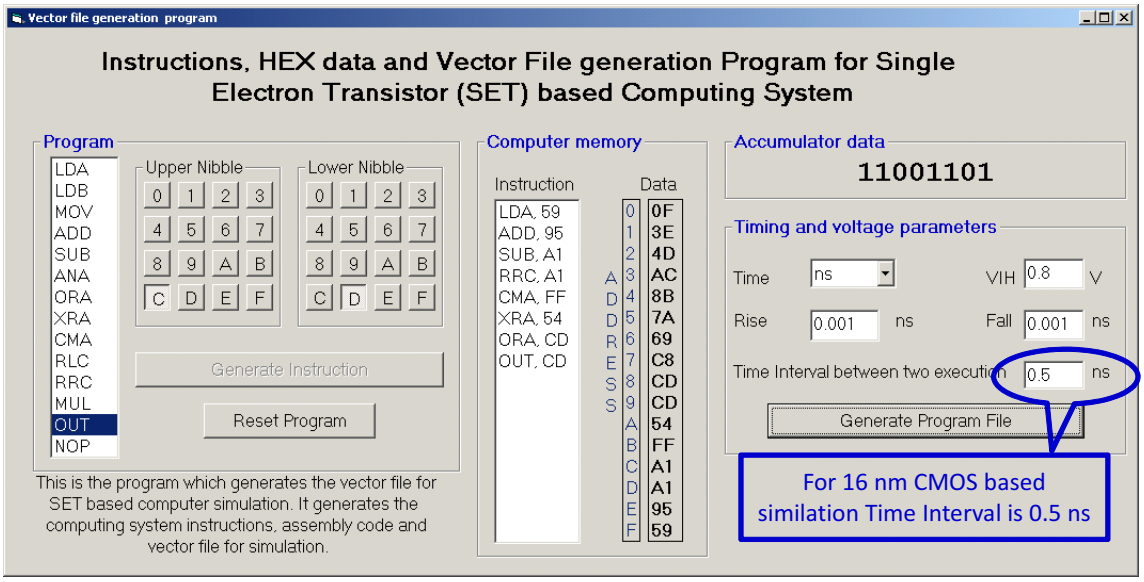


Figure 5.6: The GUI of vector file generation of code for 16 nm CMOS based computing system.

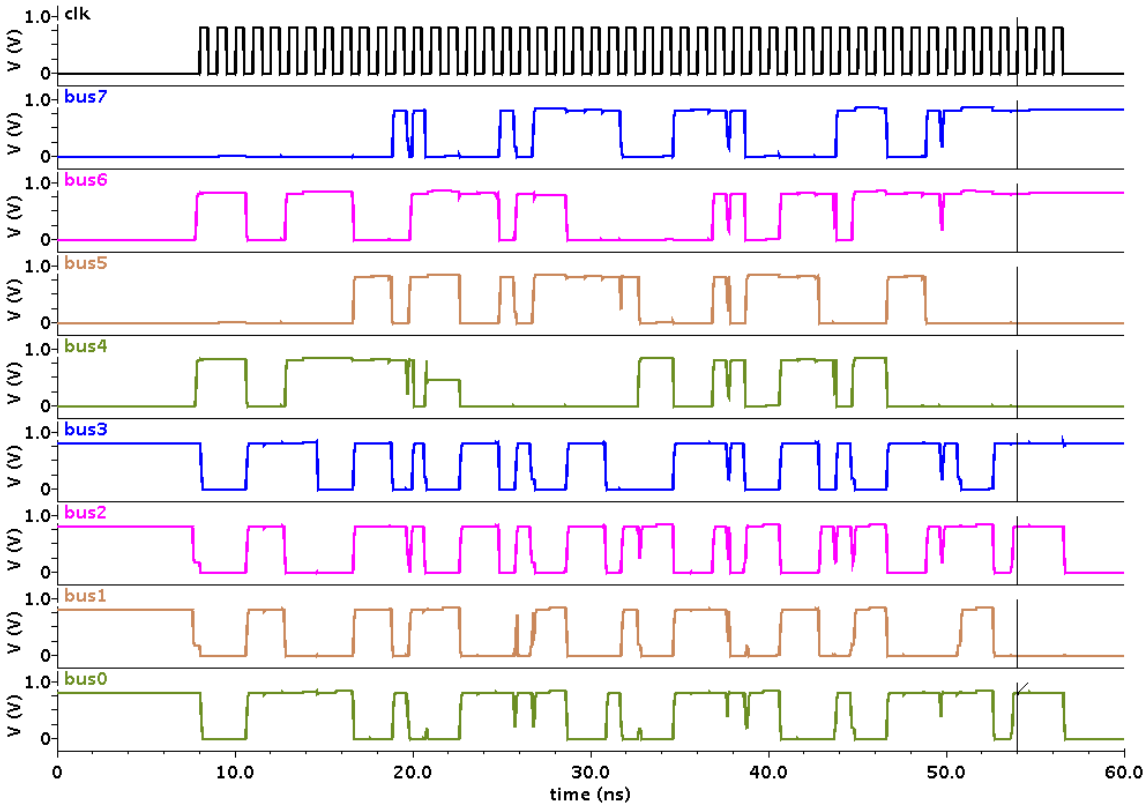


Figure 5.7: The transient analysis of 16 nm CMOS based computing system at 1 GHz for instructions as per Table 5.3.

5.5 Performance comparison of SET and 16 nm CMOS computing systems

In this section, the performance comparison of the developed computing system using conventional 16 nm CMOS technology and proposed SET is made. The 16 nm CMOS technology based computing system is designed using the same method in Cadence Virtuoso tool-set and its simulation is also carried out with the same vector files, that are used for the SET based computing system.

Table 5.4: Performance comparison of computing systems

Parameter	**SET technology**	**16 nm CMOS technology**
Max. operating frequency	5 GHz	1 GHz
Power (μW) at 1 GHz	2.570	4.092
Instructions per second	833 MIPS	166 MIPS

Table 5.4 shows the comparison of both the 16 nm CMOS and SET computing systems for operating frequency, power and instructions per second (IPS). It shows that the maximum operating frequency of 16 nm CMOS and SET based computing systems are 1 GHz and 5 GHz respectively. Hence, SET based system has appreciably (nearly 5 times) higher operating frequency. From the table it is analyzed that, the power requirement for 16 nm CMOS and SET computing systems are 4.092 μW and 2.570 μW at the operating frequency of 1 GHz respectively. It reveals that SET consumes nearly 1.6 times lesser average power dissipation and hence it is more power efficient. The IPS is calculated based on the 6-clock cycles per instruction. It is analyzed that IPS for 16 nm CMOS and SET based computing systems are 166 and 833 MIPS respectively. Hence, throughput and execution time of SET is considerably higher than 16 nm CMOS based computing system. The several analyses in this work reveal that SET performs considerably better than its counterpart 16 nm CMOS technology. It is robust against process variations and gives faithful output for all set of logic and high computing operations. Hence, SET based systems are very prominent to attain high performance system.

5.6 Variability analysis of SET based computing system

Table 5.5 lists the delay and average power dissipation of the computing system during various test conditions. It is seen from the table that variation of process parameters to $\pm$10% from its nominal values results in no difference in delay and average power dissipation of SET computing system. These measurements are carried out by Cadence waveform viewer and calculator tool. Fig. 3.1 shows the architecture of the SET based computing system where, 'Bus [7:0]' connects intermediate data among various circuit blocks through tri-state buffers. The internal two transistors of a tri-state buffer enable/disable the output. The output of tri-state buffer is connected to interconnect capacitance of 0.224 aF. The transition on 'Bus [7:0]' charge/discharge the interconnect capacitance that will propagate as delay. The delay reported in Table 5.5 indicates the time difference between clock and transition on 'Bus [7:0]' at 50% threshold values. The major factors affecting the delay are tri-state buffer enable and interconnect capacitance. In addition to, the power consumption is product of supply voltage and average current for execution of 8 instructions as mentioned in Table 5.3. Now, the variation in SET parameters (C_s, C_d, C_g, C_b, R_d and R_s) and applied voltages (V_{ds}, V_{gs} and V_{bs}) changes in I_{ds}. However, the effect of I_{ds} variation due to SET parameters change is negligible compared to tri-state buffer enable and interconnect capacitance. Consequently, the process variation effect on delay and average power consumptions measurements are negligible and not changing in the Table 5.5. Hence, this infers that the SET based computing systems are prone to process variation effects on delay and average power consumptions, and therefore good for practical implementation of high-end applications. However, SET based systems are affected by voltage and temperature variations. It is seen from the table that shift in temperature to $\pm$10% from its nominal values, results in marginal $\pm$3% variation in output performance of SET computing system. From the table, it is envisaged that the variation of supply voltage to $\pm$10% results in nearly 2 times change in the performance of SET computing system. The high variation of SET output performance with voltage can be mitigated by applying voltage regulation techniques and incorporating special DC/DC converters as a power source [124, 125]. The reason for this change is due to the existing SET process parameters optimization for the design operation at 0.8 V supply voltage. However, there is a different set of SET process parameters available for $\pm$10% supply voltage, which may give optimum performance.

Table 5.5: Parametric PVT variations for SET based computing system

Type of the Parameter	**Name of the parameter**	**Under Nominal Condition**			**Under Altered Condition**		
		Parameter Value	**Delay (ps)**	**Power (μW)**	**Parameter Value**	**Delay (ps)**	**Power (μW)**
Process	Control gate capacitance	C_g = 0.05 aF	108.8	2.522	C_g = 0.045 aF (-10%) C_g = 0.055 aF (10%)	108.8	2.522
	Tuning gate capacitance	C_b = 0.045 aF			C_b = 0.040 aF (-10%) C_b = 0.049 aF (10%)		
	Junction capacitance at the source	C_s = 0.03 aF			C_s = 0.027 aF (-10%) C_s = 0.033 aF (10%)		
	Junction capacitance at the drain	C_d = 0.03 aF			C_d = 0.027 aF (-10%) C_d = 0.033 aF (10%)		
	Tunnel resistance at the source	R_s = 1 MΩ			R_s = 0.9 MΩ (-10%) R_s = 1.1 MΩ (10%)		
	Tunnel resistance at the drain	R_d = 1 MΩ			R_d = 0.9 MΩ (-10%) R_d = 1.1 MΩ (10%)		
Voltage	supply Voltage	V_{dd} = 0.8 V	108.8	2.522	V_{dd} = 0.72 V (-10%) V_{dd} = 0.88 V (10%)	222.0 69.18	0.658 7.333
Temperature	Operating Temperature	T = 27 °C	108.8	2.522	T = 24.3 °C (-10%) T = 29.7 °C (10%)	112.0 105.6	2.440 2.606

CHAPTER 6

Conclusion

Present IC technology has grown tremendously over the last few decades by scaling of device dimensions. However, the scaling has resulted in non-ideal issues like short channel effect, power dissipation, leakage current, and process variation in MOSFET technology. To overcome these, the researchers have explored several nano-devices that deliver better performance in terms of speed and power dissipation. The SET is one of the nano-devices which attributes superior performance than the widely used MOSFET technology. In the present thesis, an extensive literature review has been carried out for SET based research in the areas of modeling, fabrication, and logic designs. The literature review shows that the SET can be heterogeneously 3D integrated to the vastly adopted CMOS technology. This is feasible by the virtue of the SET realization using BEOL fabrication process. Apart from this, the latest fabrication technology enables SET to operate at room temperature and 0.8 V supply voltage which is compatible to nano-CMOS operating range. Various researchers have carried out hybrid and standalone designs by SET-MOSFET and SET technologies respectively. The several research works demonstrate that the preliminary designs have been carried out using SET technology. However, there is a need for realizing complex designs by SET.

In the proposed work a novel 8-bit SET based computing system is implemented that operates at room temperature. Also, it works at 0.8 V which opens up 3D integration flexibility to nano-CMOS technology with existing designs. The developed design duly incorporates practical interconnect parasitic capacitances.The SET based computing system is capable of executing 14 instructions. The functionality of the computing system is verified by vector files that comprises of multiple instructions bundled in a program. The circuit diagram, test bench model and output waveforms of all the combinational and sequential components of the computing system are presented. Further, maximum delay

and power dissipation in each of these circuit designs are analyzed. For accessing the efficiency of the proposed SET based computing system, its performance is compared with conventional 16-nm CMOS technology. The SET and 16 nm CMOS computing systems operates at 1 GHz and 5 GHz with the power dissipation of 4.092 μW and 2.570 μW (at 1 GHz) respectively. The analysis reveals that SET performs considerably better with higher operating frequency (around 5 times), lower power dissipation (around 1.6 times) and higher execution of instruction per second (around 5 times) than its counterpart 16 nm CMOS technology.

At the analysis part, the performed model compatibility analysis shows that the formulated analytical model results of SET match very closely with simulation model results. To check the robustness of the SET based computing system, variability analysis has been performed. It is observed that SET based computing system is less immune to supply voltage variations. This can be compensated by applying suitable voltage regulation techniques. On the other hand for temperature and process variations, it is envisaged that the SET based computing system is very robust. Hence, it is inferred that variability issues are very lesser in SET based systems and can be good alternative to replace conventional systems.

The design of SET based computing system, verification and various analyses in the proposed work promisingly show that SET based systems are highly efficient and hence very effective to incorporate in next-generation IC designs. The integrated system with SET technology can deliver much higher performance in terms of speed, power, density, thermal budget, footprint, and functionality.

Future Prospects

The short-term perspectives for the proposed work are at design level. The proposed computing system is capable to execute 14 instructions that can be extended for further instructions. At the architecture level the design can be explored to state-of-the art present and future processor architectures. The present design has 4-bit multiplier that may be enhanced for higher bits. The medium-term perspectives for the proposed work are at fabrication level and tools development. Up till now, SET based circuits are fabricated at block level. The fabrication level of work can be carried out for SET based complex designs using foundry level support. There is unavailability of tools such that EDA tools, synthesizer, place and route tool, static timing analysis tool etc. With the support of tools and fabrication facility will initiate SET based physical higher order designs.

Publications

- **Journals:**

  1. R. Patel, Y. Agrawal, and R. Parekh, "Single-electron transistor: Review in perspective of theory, modelling, design and fabrication," *Springer Microsystem Technologies*, 2020, doi: 10.1007/s00542-020-05002-5. Citescore-3.1, (SCI Indexed).
  2. R. Patel, Y. Agrawal, and R. Parekh, "Design of prominent SET based high performance computing system," *IET Circuits, Devices and Systems*, vol. 14, no. 2, pp. 159-167, 2020, doi: 10.1049/iet-cds.2019.0166. Citescore-2.1, (SCI Indexed).
  3. R. Patel, Y. Agrawal, and R. Parekh, "Novel slice-based high-performance ALU design using prospective single electron transistor," *IETE Journal of Research*, doi: 10.1080/03772063.2019.1642803. Citescore-2.0, (SCIE Indexed).
  4. R. Patel, Y. Agrawal, and R. Parekh, "A new tool for simulation of single electron transistor based microprocessor using vector file," *Nanoscience and Nanotechnology-Asia*, vol. 10, no. 4, pp. 493-500, 2020, doi: 10.2174/2210681209666191014122904. Citescore-0.7, (Scopus Indexed).

- **Conferences:**

  1. R. Patel, Y. Agrawal, and R. Parekh, "A Vector file generation program for simulating single electron transistor based computing system," in Proc. *IEEE Electron Devices Kolkata Conference (EDKCON)*, Kolkata, India, pp. 647-650, 2018, doi: 10.1109/EDKCON.2018.8770464.
  2. R. Patel and R. Parekh, "DNA based hybrid circuit design approaches," in Proc. *IEEE International Conference on Convergence of Technology (I2CT)*, pp. 1-6, 2018, doi: 10.1109/I2CT45611.2019.9034066.

Appendix A

List of Vector Files

This section shows various vector files for transient analysis which are associated for SET based design blocks. The consecutive lines (for signal generations) in the vector file are split in multiple columns in this Annexure.

A.1 Vector file for AL slice transient analysis

```
RADIX 111111111
VNAME sel_neg sel_op1 sel_op2 shift_r force_carry1 A B Anext Carry_Prev
IO IIIIIIIII
TUNIT ns
TRISE 0.0001
TFALL 0.0001
PERIOD 1
VIH 0.8
01000 0 0 0 1  11000 0 0 0 1  01101 0 0 0 0  01001 0 0 0 1  00111 0 0 1 0
01000 0 1 0 1  11000 0 1 0 1  01101 0 1 0 0  01001 0 1 0 1  00111 0 1 1 0
01000 1 0 0 1  11000 1 0 0 1  01101 1 0 0 0  01001 1 0 0 1  00111 1 0 1 0
01000 1 1 0 1  11000 1 1 0 1  01101 1 1 0 0  01001 1 1 0 1  00111 1 1 1 0
01000 0 0 0 0  11000 0 0 0 0  00001 0 0 0 1  00111 0 0 0 0  01001 0 1 0 1
01000 0 1 0 0  11000 0 1 0 0  00001 0 1 0 1  00111 0 1 0 0  01001 1 1 0 1
01000 1 0 0 0  11000 1 0 0 0  00001 1 0 0 1  00111 1 0 0 0
01000 1 1 0 0  11000 1 1 0 0  00001 1 1 0 1  00111 1 1 0 0
```

A.2 Vector file for multiplier transient analysis

```
RADIX 4 4
VNAME a[3:0] b[3:0]
IO II
TUNIT ns
TRISE 0.001
TFALL 0.001
PERIOD 1
VIH 0.8
00        22        44        66        88        AA        CC        EE
11        33        55        77        99        BB        DD        FF
```

A.3 Vector file for 4-bit counter transient analysis

```
RADIX 1111 11 11 1
VNAME d0 d1 d2 d3 pre_ clr_ load en clk
IO IIII II II I
TUNIT ns
TRISE 0.001
TFALL 0.001
PERIOD 1
VIH 0.8
1010 11 01 0    1010 01 01 0    1010 11 01 0    1010 11 01 0    1010 11 00 0
1010 11 01 1    1010 01 01 1    1010 11 01 1    1010 11 01 1    1010 11 00 1
1010 11 01 0    1010 11 01 0    1010 11 01 0    1010 11 01 0    1010 11 00 0
1010 11 01 1    1010 11 01 1    1010 11 01 1    1010 11 01 1    1010 11 00 1
1010 10 01 0    1010 11 01 0    1010 11 01 0    1010 11 01 0    1010 11 00 0
1010 10 01 1    1010 11 01 1    1010 11 01 1    1010 11 01 1    1010 11 00 1
1010 11 01 0    1010 11 01 0    1111 11 11 0    1010 11 01 0    1010 11 00 0
1010 11 01 1    1010 11 01 1    1111 11 11 1    1010 11 01 1    1010 11 00 1
1010 11 01 0    1010 11 01 0    1010 11 01 0    1010 11 00 0    1010 11 01 0
1010 11 01 1    1010 11 01 1    1010 11 01 1    1010 11 00 1    1010 11 01 1
```

```
1010 11 01 0    1010 11 01 0    1010 11 01 0    1010 11 01 0    1010 11 01 0
1010 11 01 1    1010 11 01 1    1010 11 01 1    1010 11 01 1    1010 11 01 1
1010 11 01 0    1010 11 01 0    1010 11 01 0    1010 11 01 0    1010 11 01 0
1010 11 01 1    1010 11 01 1    1010 11 01 1    1010 11 01 1    1010 11 01 1
1010 11 01 0    1010 11 01 0    1010 11 01 0    1010 11 01 0    1010 11 01 0
1010 11 01 1    1010 11 01 1    1010 11 01 1    1010 11 01 1    1010 11 01 1
1010 11 01 0    1010 11 01 0    1010 11 01 0    1010 11 01 0    1010 11 01 0
1010 11 01 1    1010 11 01 1    1010 11 01 1    1010 11 01 1    1010 11 01 1
1010 11 01 0    1010 11 01 0    1010 11 01 0    1010 11 01 0    1010 11 01 0
1010 11 01 1    1010 11 01 1    1010 11 01 1    1010 11 01 1    1010 11 01 1
```

A.4 Vector file for 4-bit register transient analysis

```
RADIX 111 4
VNAME load clr clk d[3:0]
IO III I
TUNIT ns
TRISE 0.001
TFALL 0.001
PERIOD 1
VIH 0.8
000 0     110 A     000 0     110 1     000 0     110 F
001 0     111 A     001 0     111 1     001 0     111 F
010 0     010 0     010 0     010 0     010 0     010 0
011 0     011 0     011 0     011 0     011 0     011 0
```

A.5 Vector file for controller transient analysis

```
RADIX 4 1 1
VNAME bit[7:4] clk clr_
IO I I I
TUNIT ns
TRISE 0.001
```

```
TFALL 0.001
PERIOD 1
VIH 0.8
0 0 0    1 0 1    3 0 1    5 0 1    7 0 1    8 0 1    A 0 1    C 0 1
0 1 0    1 1 1    3 1 1    5 1 1    7 1 1    8 1 1    A 1 1    C 1 1
0 0 0    1 0 1    3 0 1    5 0 1    7 0 1    9 0 1    A 0 1    C 0 1
0 1 0    1 1 1    3 1 1    5 1 1    7 1 1    9 1 1    A 1 1    C 1 1
0 0 1    1 0 1    3 0 1    5 0 1    7 0 1    9 0 1    B 0 1    C 0 1
0 1 1    1 1 1    3 1 1    5 1 1    7 1 1    9 1 1    B 1 1    C 1 1
0 0 1    2 0 1    3 0 1    5 0 1    7 0 1    9 0 1    B 0 1    D 0 1
0 1 1    2 1 1    3 1 1    5 1 1    7 1 1    9 1 1    B 1 1    D 1 1
0 0 1    2 0 1    4 0 1    5 0 1    7 0 1    9 0 1    B 0 1    D 0 1
0 1 1    2 1 1    4 1 1    5 1 1    7 1 1    9 1 1    B 1 1    D 1 1
0 0 1    2 0 1    4 0 1    6 0 1    7 0 1    9 0 1    B 0 1    D 0 1
0 1 1    2 1 1    4 1 1    6 1 1    7 1 1    9 1 1    B 1 1    D 1 1
0 0 1    2 0 1    4 0 1    6 0 1    8 0 1    9 0 1    B 0 1    D 0 1
0 1 1    2 1 1    4 1 1    6 1 1    8 1 1    9 1 1    B 1 1    D 1 1
0 0 1    2 0 1    4 0 1    6 0 1    8 0 1    A 0 1    B 0 1    D 0 1
0 1 1    2 1 1    4 1 1    6 1 1    8 1 1    A 1 1    B 1 1    D 1 1
1 0 1    2 0 1    4 0 1    6 0 1    8 0 1    A 0 1    C 0 1    D 0 1
1 1 1    2 1 1    4 1 1    6 1 1    8 1 1    A 1 1    C 1 1    D 1 1
1 0 1    3 0 1    4 0 1    6 0 1    8 0 1    A 0 1    C 0 1
1 1 1    3 1 1    4 1 1    6 1 1    8 1 1    A 1 1    C 1 1
1 0 1    3 0 1    5 0 1    6 0 1    8 0 1    A 0 1    C 0 1
1 1 1    3 1 1    5 1 1    6 1 1    8 1 1    A 1 1    C 1 1
```

A.6 Vector file for SET and 16 nm CMOS based computing system transient analysis

```
; ---------------------
; Vector file for SET based Computing System Testing
; Date:  23-03-2021 Time:  06:48:30 AM
; Generated from VB Program
```

```
; SAC / DAIICT
; Ahmedabad / Gandhinagar
; ---------------------
RADIX 44 4444 1 1
vname bl[7:0] wl[15:0] clr clk
IO II IIII I I
TUNIT ns
TRISE 0.001
TFALL 0.001
PERIOD 0.1
VIH 0.8
; ---------------------
;The output 11001101 is available at 10.8ns
; ---------------------
;

These blue lines are applicable for 16 nm cmos based computing systems
simulation
PERIOD 0.5
VIH 0.8
; ---------------------
;The output 11001101 is available at 54ns
; ---------------------
0F 0001 1 0
3E 0002 1 0
4D 0004 1 0
AC 0008 1 0
8B 0010 1 0
7A 0020 1 0
69 0040 1 0
C8 0080 1 0
CD 0100 1 0
CD 0200 1 0
```

```
54 0400 1 0
FF 0800 1 0
A1 1000 1 0
A1 2000 1 0
95 4000 1 0
59 8000 1 0
; ---------------------
;Config OVER; uP Reset Start
00 0000 0 1
00 0000 0 0
;uP is Reset; Program in RUN
; ---------------------
; LDA, 59
00 0000 1 1
00 0000 1 0
00 0000 1 1
00 0000 1 0
00 0000 1 1
00 0000 1 0
00 0000 1 1
00 0000 1 0
00 0000 1 1
00 0000 1 0
00 0000 1 1
00 0000 1 0
; ---------------------
; ADD, 95
00 0000 1 1
00 0000 1 0
00 0000 1 1
00 0000 1 0
00 0000 1 1
00 0000 1 0
```

```
00 0000 1 1
00 0000 1 0
00 0000 1 1
00 0000 1 0
00 0000 1 1
00 0000 1 0
; ---------------------
; SUB, A1
00 0000 1 1
00 0000 1 0
00 0000 1 1
00 0000 1 0
00 0000 1 1
00 0000 1 0
00 0000 1 1
00 0000 1 0
00 0000 1 1
00 0000 1 0
00 0000 1 1
00 0000 1 0
; ---------------------
; RRC, A1
00 0000 1 1
00 0000 1 0
00 0000 1 1
00 0000 1 0
00 0000 1 1
00 0000 1 0
00 0000 1 1
00 0000 1 0
00 0000 1 1
00 0000 1 0
00 0000 1 1
```

```
00 0000 1 0
; ---------------------
; CMA, FF
00 0000 1 1
00 0000 1 0
00 0000 1 1
00 0000 1 0
00 0000 1 1
00 0000 1 0
00 0000 1 1
00 0000 1 0
00 0000 1 1
00 0000 1 0
00 0000 1 1
00 0000 1 0
; ---------------------
; XRA, 54
00 0000 1 1
00 0000 1 0
00 0000 1 1
00 0000 1 0
00 0000 1 1
00 0000 1 0
00 0000 1 1
00 0000 1 0
00 0000 1 1
00 0000 1 0
00 0000 1 1
00 0000 1 0
; ---------------------
; ORA, CD
00 0000 1 1
00 0000 1 0
```

```
00 0000 1 1
00 0000 1 0
00 0000 1 1
00 0000 1 0
00 0000 1 1
00 0000 1 0
00 0000 1 1
00 0000 1 0
00 0000 1 1
00 0000 1 0
; ---------------------
; OUT, CD
00 0000 1 1
00 0000 1 0
00 0000 1 1
00 0000 1 0
00 0000 1 1
00 0000 1 0
00 0000 1 1
00 0000 1 0
00 0000 1 1
00 0000 1 0
00 0000 1 1
00 0000 1 0
```

Appendix B

Tool Source Code

This appendix shows the Visual Basic source code for the developed vector file generation tool. The tool GUI with control names (shown with magenta text) is shown in Fig. B.1.

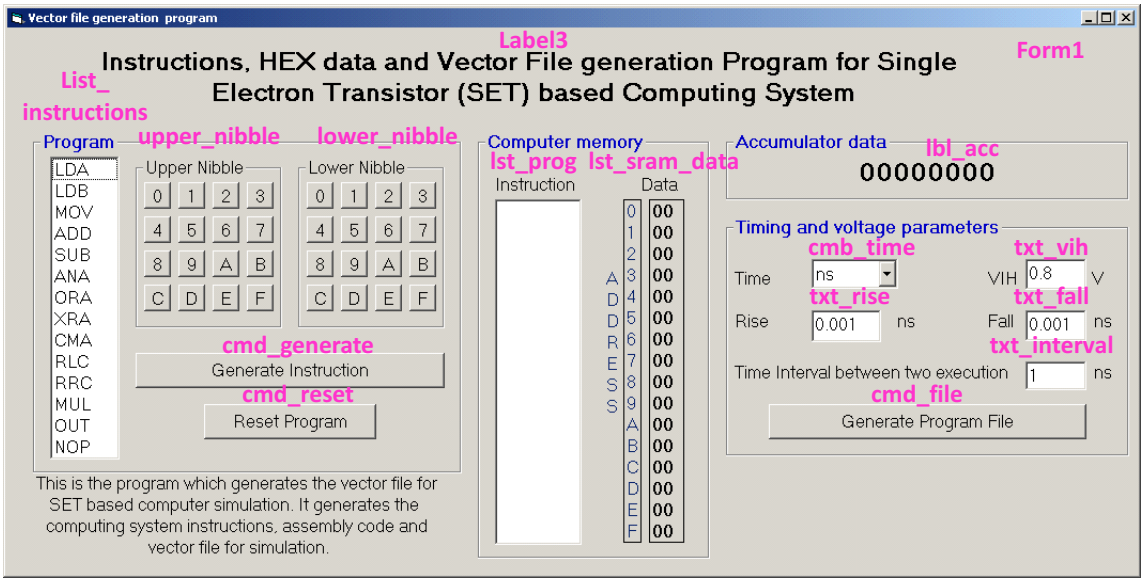


Figure B.1: The GUI of vector file generation of code with control names.

```
  Public upper_nibble_checked As Integer
Public write_instruction_index As Integer
Public write_data_index As Integer
Public no_of_instruction As Integer
Dim opcode As String
Public op_data As String
Public op_data_writen As Boolean

Public Function lda(a As String) As String
lda = a
End Function
Public Function ana(a As String, b As String) As String
Dim len_a As Integer
Dim len_b As Integer
```

```
Dim char_a, char_b As String
Dim op_s As String
ops = ""
len_a = Len(a)
len_b = Len(b)
For i = 1 To len_a
   char_a = Mid(a, i, 1)
   char_b = Mid(b, i, 1)
   Select Case char_a & char_b
      Case "00"
         op_s = op_s & 0
      Case "01"
         op_s = op_s & 0
      Case "10"
         op_s = op_s & 0
      Case Else
         op_s = op_s & 1
   End Select
Next
ana = op_s
End Function

Public Function ora(a As String, b As String) As String
Dim len_a As Integer
Dim len_b As Integer
Dim char_a, char_b As String
Dim op_s As String
ops = ""
len_a = Len(a)
len_b = Len(b)
For i = 1 To len_a
   char_a = Mid(a, i, 1)
   char_b = Mid(b, i, 1)
   Select Case char_a & char_b
      Case "00"
         op_s = op_s & 0
   Case "01"
      op_s = op_s & 1
   Case "10"
      op_s = op_s & 1
   Case Else
      op_s = op_s & 1
   End Select
Next
ora = op_s
End Function

Public Function xra(a As String, b As String) As String
Dim len_a As Integer
Dim len_b As Integer
```

```
Dim char_a, char_b As String
Dim op_s As String
ops = ""
len_a = Len(a)
len_b = Len(b)
For i = 1 To len_a
  char_a = Mid(a, i, 1)
  char_b = Mid(b, i, 1)
  Select Case char_a & char_b
  Case "00"
    op_s = op_s & 0
  Case "01"
    op_s = op_s & 1
  Case "10"
    op_s = op_s & 1
  Case Else
    op_s = op_s & 0
  End Select
Next
xra = op_s
End Function

Public Function cma(a As String) As String
Dim len_a As Integer

Dim char_a As String
Dim op_s As String
ops = ""
len_a = Len(a)
For i = 1 To len_a
  char_a = Mid(a, i, 1)
  Select Case char_a
  Case "0"
    op_s = op_s & 1
  Case Else
    op_s = op_s & 0
  End Select
Next
cma = op_s
End Function

Public Function add(a As String, b As String, c As String) As String
Dim len_a As Integer
Dim len_b As Integer
Dim char_a, char_b As String
Dim op_s As String
ops = ""
len_a = Len(a)
len_b = Len(b)
For i = len_a To 1 Step -1
```

```
  char_a = Mid(a, i, 1)
  char_b = Mid(b, i, 1)
  Select Case char_a & char_b & c
  Case "000"
    op_s = 0 & op_s
    c = "0"
  Case "001"
    op_s = 1 & op_s
    c = "0"
  Case "010"
    op_s = 1 & op_s
    c = "0"
  Case "011"
    op_s = 0 & op_s
    c = "1"
  Case "100"
    op_s = 1 & op_s
    c = "0"
  Case "101"
    op_s = 0 & op_s
    c = "1"
  Case "110"
    op_s = 0 & op_s
    c = "1"
  Case Else
    op_s = 1 & op_s
    c = "1"
  End Select
Next
add = op_s
End Function

Public Function sbb(a As String, b As String, c As String) As String
Dim len_a As Integer
Dim len_b As Integer
Dim char_a, char_b As String
Dim op_s As String
ops = ""
len_a = Len(a)
len_b = Len(b)
For i = len_a To 1 Step -1
  char_a = Mid(a, i, 1)
  char_b = Mid(b, i, 1)
  Select Case char_a & char_b & c
  Case "000"
    op_s = 0 & op_s
    c = "0"
  Case "001"
    op_s = 1 & op_s
    c = "1"
```

```
  Case "010"
    op_s = 1 & op_s
    c = "1"
  Case "011"
    op_s = 0 & op_s
    c = "1"
  Case "100"
    op_s = 1 & op_s
    c = "0"
  Case "101"
    op_s = 0 & op_s
    c = "0"
  Case "110"
    op_s = 0 & op_s
    c = "0"
  Case Else
    op_s = 1 & op_s
    c = "1"
  End Select
Next
sbb = op_s
End Function

Public Function rlc(a As String) As String
Dim len_a As Integer
Dim op_s As String
len_a = Len(a)
op_s = Mid(a, 2, len_a) & 0 ' abcd => bcd0
rlc = op_s
End Function

Public Function rrc(a As String) As String
Dim len_a As Integer
Dim op_s As String
len_a = Len(a)
op_s = 0 & Mid(a, 1, len_a - 1) ' abcd => 0abc
rrc = op_s
End Function

Public Function mul(a As String, b As String) As String
Dim len_a As Integer
Dim len_b As Integer
Dim char_a, char_b As String
Dim op_s As String
Dim modified_a As String
Dim modified_b As String
Dim p As String
p = "00000000"
modified_a = "0000" & a
modified_b = "0000" & b
```

```
ops = ""
len_a = Len(a)
len_b = Len(b)
If Mid(modified_b, 8, 1) = 1 Then
  op_s = modified_a
Else
  op_s = "00000000"
End If
If Mid(modified_b, 7, 1) = 1 Then
  p = rlc(modified_a)
Else
  p = "00000000"
End If
op_s = add(p, op_s, 0)
If Mid(modified_b, 6, 1) = 1 Then
  p = rlc(modified_a)
  p = rlc(p)
Else
  p = "00000000"
End If
op_s = add(p, op_s, 0)
If Mid(modified_b, 5, 1) = 1 Then
  p = rlc(modified_a)
  p = rlc(p)
  p = rlc(p)
Else
  p = "00000000"
End If
op_s = add(p, op_s, 0)
mul = op_s
End Function

Public Function out(a As String) As String
out = a
End Function

Public Function nop(a As String) As String
nop = a
End Function

Public Function hex2bin(a As String) As String
Select Case a
  Case "0"
  s = "0000"
  Case "1"
  s = "0001"
  Case "2"
  s = "0010"
  Case "3"
  s = "0011"
```

```
   Case "4"
   s = "0100"
   Case "5"
   s = "0101"
   Case "6"
   s = "0110"
   Case "7"
   s = "0111"
   Case "8"
   s = "1000"
   Case "9"
   s = "1001"
   Case "A"
   s = "1010"
   Case "B"
   s = "1011"
   Case "C"
   s = "1100"
   Case "D"
   s = "1101"
   Case "E"
   s = "1110"
   Case Else
   s = "1111"
End Select
hex2bin = s
End Function

Private Sub cmd_file_Click()
Dim op_available_time As Double
Dim op_s As String

Text1.Text = "d:
Prog" & Format(Now, "DDMMYYhmmss") & ".txt"
Open Text1.Text For Output As #1   ' Open file for output.
Print #1, "; ---------------------"   ' Print text to file.
Print #1, "; Vector file for SET based Computing System Testing"   ' Print
text to file.
Print #1, ";     Date:  " & Date & " Time:  " & Time
Print #1, ";     Generated from VB Program "   ' Print text to file.
Print #1, ";          SAC / DAIICT"   ' Print five leading spaces.
Print #1, ";     Ahmedabad / Gandhinagar" ' Print word at column 10.
Print #1, "; ---------------------"   ' Print text to file.

Print #1, "RADIX 44 4444 1 1"
Print #1, "vname bl[7:0] wl[15:0] clr clk"
Print #1, "IO II IIII I I"
Print #1, "TUNIT " & cmb_time.Text
Print #1, "TRISE " & txt_rise.Text
Print #1, "TFALL " & txt_fall.Text
```

```
Print #1, "PERIOD " & txt_interval.Text
Print #1, "VIH " & txt_vih.Text
op_available_time = 0
op_available_time = 18 * Val(txt_interval.Text) '16 instructions + 1 reset
clock (1 high and 1 low so total 2)
'If op_data_writen = True Then
  For i = 0 To no_of_instruction - 1
    lst_prog.ListIndex = i
    If Mid(lst_prog.Text, 1, 3) = "OUT" Then
      op_available_time = op_available_time + 6 * Val(txt_interval.Text)
'for OUT 3 T staes and op is available at half time of T4 state
      Print #1, "; ---------------------"   ' Print text to file.
      Print #1, ";The output " & op_data & " is available at " &
op_available_time & cmb_time.Text
      Print #1, "; ---------------------"   ' Print text to file.
      Exit For
    End If
    op_available_time = op_available_time + 12 * Val(txt_interval.Text)
'each execution 6 T-states (so, 1 High and 1 low)
  Next
'   op_data_writen = False
'End If

  For i = 0 To 15
  lst_sram_data.ListIndex = i
  Select Case i
    Case 0:  Print #1, lst_sram_data.Text & " 0001 1 0"
    Case 1:  Print #1, lst_sram_data.Text & " 0002 1 0"
    Case 2:  Print #1, lst_sram_data.Text & " 0004 1 0"
    Case 3:  Print #1, lst_sram_data.Text & " 0008 1 0"
    Case 4:  Print #1, lst_sram_data.Text & " 0010 1 0"
    Case 5:  Print #1, lst_sram_data.Text & " 0020 1 0"
    Case 6:  Print #1, lst_sram_data.Text & " 0040 1 0"
    Case 7:  Print #1, lst_sram_data.Text & " 0080 1 0"
    Case 8:  Print #1, lst_sram_data.Text & " 0100 1 0"
    Case 9:  Print #1, lst_sram_data.Text & " 0200 1 0"
    Case 10:  Print #1, lst_sram_data.Text & " 0400 1 0"
    Case 11:  Print #1, lst_sram_data.Text & " 0800 1 0"
    Case 12:  Print #1, lst_sram_data.Text & " 1000 1 0"
    Case 13:  Print #1, lst_sram_data.Text & " 2000 1 0"
    Case 14:  Print #1, lst_sram_data.Text & " 4000 1 0"
    Case Else:  Print #1, lst_sram_data.Text & " 8000 1 0"
  End Select
  Next i
  Print #1, "; ---------------------"   ' Print text to file.
  Print #1, ";Config OVER; uP Reset Start"
  Print #1, "00 0000 0 1"
  Print #1, "00 0000 0 0"
  Print #1, ";uP is Reset; Program in RUN"
  For i = 0 To no_of_instruction - 1
```

```
   lst_prog.ListIndex = i
   Print #1, "; ---------------------"   ' Print text to file.
   Print #1, "; " & lst_prog.Text
   For j = 0 To 5
        Print #1, "00 0000 1 1"
        Print #1, "00 0000 1 0"
   Next
   Next

   Close #1
   status = MsgBox("File Generated Successfully.  Do you want to Open?",
vbYesNo)
   If status = 6 Then
   op_s = "notepad " & Text1.Text
   i = Shell(op_s, vbNormalFocus)
   End If
   If status = 7 Then

   cmd_reset_Click
   End If
End Sub


Private Sub cmd_generate_Click()
Dim acc_data As String
no_of_instruction = no_of_instruction + 1
Text2.Text = list_instructions.ListIndex
'GENERATE PROGRAM (INSTRUCTIONS)
'EX. LDA, 35; CMA, FF
'0     1     2     3     4     5     6     7     8     9     A     B     C     D
'LDA   LDB   MOV   ADD   SUB   ANA   ORA   XRA   CMA   RLC   RRC   MUL   OUT   NOP

Select Case list_instructions.ListIndex
Case 8, 9, 2 'CMA 'RLC 'MOV
   Text1.Text = list_instructions.Text + ", FF"
   lst_prog.AddItem Text1.Text
Case Else
   Text1.Text = list_instructions.Text + ", " + upper_nibble(upper_nibble_checked)
   .Caption + lower_nibble(lower_nibble_checked).Caption
   lst_prog.AddItem Text1.Text
End Select

'SELECT INSTRUCTION OPCODE (UPPER NIBBLE)
'EX. FOR LDA-0; OUT-E
Select Case list_instructions.ListIndex
Case 0 To 9
   opcode = Str(list_instructions.ListIndex)
Case 10
   opcode = "A"
Case 11
```

```
   opcode = "B"
Case 12
   opcode = "C"
Case 13
   opcode = "D"
Case 14
   opcode = "E"
Case Else
   opcode = "F"
End Select

'SELECT SRAM MEMORY LOCATION (LOWER NIBBLE)
'FOR THE ADOVE OPCODE; ON WHICH ADDRESS SELECTED
'THE DATA IS WRITTEN
'AT START OF THE PROGRAM IT IS AT ADDRESS 15 THEN 14 THEN 13 AND SO ON
Select Case write_data_index
Case 0 To 9
   address = Str(write_data_index)
Case 10
   address = "A"
Case 11
   address = "B"
Case 12
   address = "C"
Case 13
   address = "D"
Case 14
   address = "E"
Case Else
   address = "F"
End Select

'WRITE ABODE UPPER AND LOWER NIBBLE TO SRAM
'OPCODE AND SRAM ADDRESS LOCATION (WHERE THE ACTUAL DATA IS STORED)
lst_sram_data.AddItem Trim(opcode) & Trim(address),
write_instruction_index   'LDA
lst_sram_data.RemoveItem (write_instruction_index + 1)
write_instruction_index = write_instruction_index + 1

'WRITE SELECTED (FROM TWO HEX BUTTON CHECKED) DATA
'ACTUAL DATA
Select Case list_instructions.ListIndex
Case 8, 9, 2 'CMA 'RLC 'MOV
   lst_sram_data.AddItem "FF", write_data_index
Case Else
   lst_sram_data.AddItem Trim(upper_nibble(upper_nibble_checked).Caption) +
Trim(lower_nibble(lower_nibble_checked).Caption), write_data_index
End Select

'MANAGE POINTERS FOR NEXT INSTRUCTION WRITING
```

```
lst_sram_data.RemoveItem (write_data_index + 1)
write_data_index = write_data_index - 1

If (write_instruction_index - write_data_index) >= 0 Then
   cmd_generate.Enabled = False
Else
   cmd_generate.Enabled = True
End If

acc_data = hex2bin(upper_nibble(upper_nibble_checked).Caption) &
hex2bin(lower_nibble(lower_nibble_checked).Caption)
Select Case list_instructions.Text
   Case "LDA"
   lbl_acc.Caption = acc_data
   Case "LDB" 'NO CHANGE IN ACC DATA
   lbl_acc.Caption = lbl_acc.Caption
   Case "MOV" 'MOV A TO B; NO CHANGE IN ACC DATA
   lbl_acc.Caption = lbl_acc.Caption
   Case "ADD"
   lbl_acc.Caption = add(lbl_acc.Caption, acc_data, 0)
   Case "SUB"
   lbl_acc.Caption = sbb(lbl_acc.Caption, acc_data, 0)
   Case "ANA"
   lbl_acc.Caption = ana(lbl_acc.Caption, acc_data)
   Case "ORA"
   lbl_acc.Caption = ora(lbl_acc.Caption, acc_data)
   Case "XRA"
   lbl_acc.Caption = xra(lbl_acc.Caption, acc_data)
   Case "CMA"
   lbl_acc.Caption = cma(lbl_acc.Caption)
   Case "RLC"
   lbl_acc.Caption = rlc(lbl_acc.Caption)
   Case "RRC"
   lbl_acc.Caption = rrc(lbl_acc.Caption)
   Case "MUL"
   lbl_acc.Caption = mul(Mid(lbl_acc.Caption, 5, 4), Mid(acc_data, 5, 4))
   Case "OUT"
   lbl_acc.Caption = out(lbl_acc.Caption)
   op_data = lbl_acc.Caption
   Case Else
   lbl_acc.Caption = out(lbl_acc.Caption)
End Select
End Sub

Private Sub cmd_reset_Click()
op = MsgBox("The SET uP Program will be erased?", vbOKCancel)

If op = 1 Then
   write_instruction_index = 0
```

```
   write_data_index = 15
   For i = 0 To 13
        list_instructions.RemoveItem (0)
   Next
   For i = 0 To 15
        upper_nibble(i).Value = False
        lower_nibble(i).Value = False
        lst_sram_addr.RemoveItem (0)
        lst_sram_data.RemoveItem (0)
   Next

   For i = 0 To no_of_instruction - 1
        lst_prog.RemoveItem (0)
   Next

   cmd_generate.Enabled = True

   form_load
End If
End Sub

Private Sub form_load()

list_instructions.AddItem "LDA"
list_instructions.AddItem "LDB"
list_instructions.AddItem "MOV"
list_instructions.AddItem "ADD"
list_instructions.AddItem "SUB"
list_instructions.AddItem "ANA"
list_instructions.AddItem "ORA"
list_instructions.AddItem "XRA"
list_instructions.AddItem "CMA"
list_instructions.AddItem "RLC"
list_instructions.AddItem "RRC"
list_instructions.AddItem "MUL"
list_instructions.AddItem "OUT"
list_instructions.AddItem "NOP"

For i = 0 To 9
   upper_nibble(i).Caption = upper_nibble(i).Index
   lower_nibble(i).Caption = lower_nibble(i).Index
Next
upper_nibble(10).Caption = "A"
upper_nibble(11).Caption = "B"
upper_nibble(12).Caption = "C"
upper_nibble(13).Caption = "D"
upper_nibble(14).Caption = "E"
upper_nibble(15).Caption = "F"
lower_nibble(10).Caption = "A"
lower_nibble(11).Caption = "B"
```

```
lower_nibble(12).Caption = "C"
lower_nibble(13).Caption = "D"
lower_nibble(14).Caption = "E"
lower_nibble(15).Caption = "F"

lst_sram_addr.AddItem "0"
lst_sram_addr.AddItem "1"
lst_sram_addr.AddItem "2"
lst_sram_addr.AddItem "3"
lst_sram_addr.AddItem "4"
lst_sram_addr.AddItem "5"
lst_sram_addr.AddItem "6"
lst_sram_addr.AddItem "7"
lst_sram_addr.AddItem "8"
lst_sram_addr.AddItem "9"
lst_sram_addr.AddItem "A"
lst_sram_addr.AddItem "B"
lst_sram_addr.AddItem "C"
lst_sram_addr.AddItem "D"
lst_sram_addr.AddItem "E"
lst_sram_addr.AddItem "F"

lst_sram_data.AddItem "00"
lst_sram_data.AddItem "00"
lst_sram_data.AddItem "00"
lst_sram_data.AddItem "00"
lst_sram_data.AddItem "00"
lst_sram_data.AddItem "00"
lst_sram_data.AddItem "00"
lst_sram_data.AddItem "00"
lst_sram_data.AddItem "00"
lst_sram_data.AddItem "00"
lst_sram_data.AddItem "00"
lst_sram_data.AddItem "00"
lst_sram_data.AddItem "00"
lst_sram_data.AddItem "00"
lst_sram_data.AddItem "00"
lst_sram_data.AddItem "00"
'   upper_nibble(5).Value = 1
'text1 is hidden text box control

no_of_instruction = 0
write_instruction_index = 0
write_data_index = 15
cmb_time.ListIndex = 0
Label3.Caption = "Instructions, HEX data and Vector File generation Program
for Single Electron Transistor (SET) based Computing System"
lbl_acc.Caption = "00000000"
op_data = ""
op_data_writen = True
```

```
End Sub

Private Sub list_instructions_Click()
   ' Text1.Text = list_instructions.ListIndex
End Sub

Private Sub list_instructions_MouseDown(Button As Integer, Shift As Integer,
x As Single, y As Single)
   'Text1.Text = Button
   'list_instructions.Drag (vbBeginDrag)
End Sub

Private Sub lst_prog_DragDrop(Source As Control, x As Single, y As Single)
   lst_prog.AddItem list_instructions.Text
End Sub

Private Sub upper_nibble_Click(Index As Integer)
   upper_nibble_checked = Index
End Sub

Private Sub lower_nibble_Click(Index As Integer)
   lower_nibble_checked = Index
End Sub
```

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